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LCD TV

Service Manual

Model: LCT-26CHSTP
Chassis: LS-08

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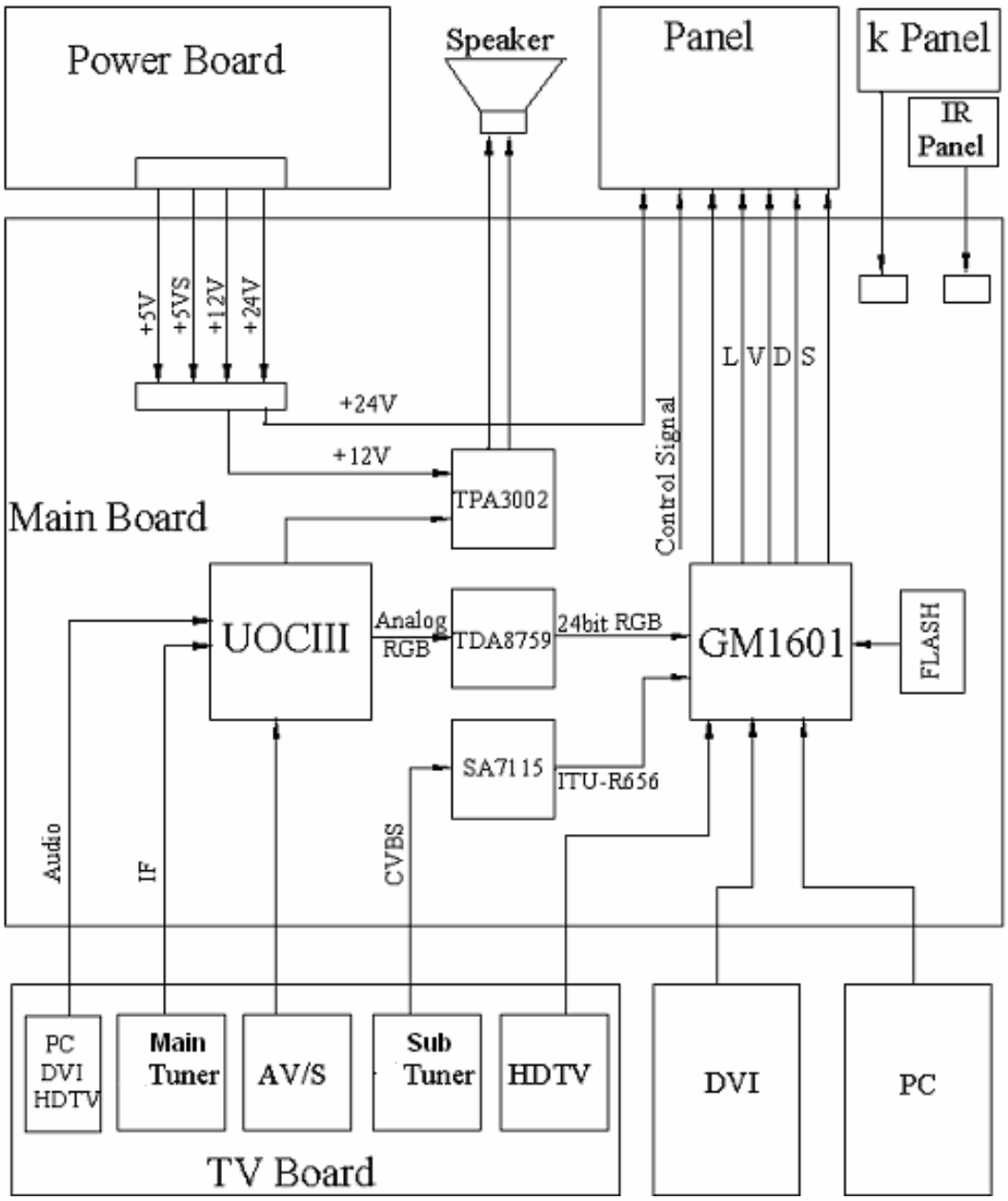
MAIN FEATURES

- Radio Frequency input; support CATV
  Capable to receive the full-append cable programs in 470MHZ
- SCART input/output
  SCART1can input CVBS/RGB Video format, SCART2 can input CVBS Video format, both can output TV signal
- AV input
  Capable to receive PAL, NTSC, SECAM color systems; Very convenient to watch VCR (video cassette recorder), Pickup Camera, other Disc's programs
- Y/C component signal input (same to S-Video input)
  Convenient to receive the Y/C high definition component signal from DVD
- HDTV input
  Capable to receive the high definition YPbPr signal in 480i, 480p, 576i, 720p, 1080i, and 1080p formats
- VGA input
  Convenient to connect with the host computer
  Capable to use as the display terminal
  Connect the 3.5mm(diameter) audio cord to your computer's audio main board, you can listening the beautiful music transmitted from your host computer
- DVI input
  Convenient to receive DVI signal
- Teletext decoder
- PIP, POP, PBP function
- Turn on with intelligence
- Zoom mode
- LTI, CTI, and black field
- BBE sound technology
- TruSurround sound technology
- Full-light display
- Picture amending display function
- Super definition display panel
- 3:2, 2:2 Pull Down
- TV program scan function
- Timer function
  Automatically on/off in certain preset time, and transmit automatically to the fixed channel
- Blue background noise reduction
  In TV, AV (S-Video), YCbCr, and YPbPr modes, screen displays soft blue background if there is no signal input

- Auto Off if no signal input
  In TV mode, the LCD TV will automatically power off within 15 minutes and enter into the Power Energy Saving Mode if there is no signal input.
- Chinese/English menu
  Ordinary and graphical user interface makes the menu operation more convenient and intuitionist
- Power Energy Saving Mode (power management mode)
  In PC mode, the LCD TV will automatically power off within 30 seconds and enter into the Power Energy Saving Mode if there is no VGA signal input. It will automatically exit from the Power Energy Saving Mode and work again when it received a valid VGA signal or press any button on the panel/remote control.
- Plug and Play
  It is no need to equip any installation software when the product is used as computer terminal display equipment
- Legerity, convenience, low power consumption

Unit IC Compositions:

LS08 chassis LCD TV is mainly composed of regulator IC, RF IC, video processor IC, Power Amplify IC, Analog Video IC, System Control IC and Key Control IC, see this IC frame as below:



PCB Assembly：

It is mainly composed of TV Board、Remote Control Receiver (Signal Receiver), K Board and Main Board. Hereunder function introduction to every PCB Assembly:

No.	Parts	Description
1	Main Board Assembly	It is the core of signal processing for LCD TV, which takes responsibility of transforming outer signal into the uniform digital signal identified by LCD display with use of System Control IC TV and AV signals input from TV Board are decoded by UOCIII to transport RGB signal which is to be transformed by TDA8759 modulus to transport 24bit RGB digital signal, then it is to be transformed by GM1601/GM1501 to produce LVDS signal displayed on the screen, in addition, signals input from VGA, DVI would directly enter into GM1501 procedure, format transformation and on screen display.
2	TV Board Assembly	It is mainly composed of two tuners (main and sub tuners), AV/S, HD signal terminals and some peripheral processing IC. The main tuner demodulates RF signal to IF signal, and the sub tuner produces CVBS signal, all signals are sent to the main board after transfer.
3	Remote Control Receiver Assembly	It is composed of one indicator light and one remote control receiver, which enable Users operate the TV conveniently and know its current working status simply with a remote control.
4	Built-in Power Board Assembly	It can transform AC 220V into DC for ICs, including +24V, +12V, +5V and +5VS power supply in standby mode.
5	K Board Assembly	It consists of 7 function buttons by which users can operate the TV freely.
6	Screen Assembly	Screens for LS08 have built-in adverse transformer, which change DC to high voltage AC signal lightening the back light; The LCD screen is used to display the image after the image signal has been processed by the main board.

MAIN ICS FUNCTION INTRODUCTION

GENERAL INTRODUCTION

TV Board			
Number	Location	Type	Main Function
1	UT1	TAD5-E2I22RW2	Audio and image intermediate frequency signal output
2	UT2	TMD2-E49IPWA	Sub picture CVBS signal output
Main Board			
3	U302, U303	24LC21A T/SN	EEPROM
4	U701	24LC32A T/SN	Buffer
5	U306, U307, UA3	FSAV330QSCX	Switch selection
6	K201	K3953M	Audio surface filter
7	K202	K9656M	Audio surface filter
8	U6	TPA3002D2PHPR	Audio amplifier
9	U801	AM29LV800DT-70EC	Flash，control program inside
10	U700	GM1501-BD	Video processor
11	U201	TDA15021H/N1B07	AV decoder
12	U402	SAA7115HL/V1	Sub channel video decoder
13	U305	SM5302AS-G-ET	High definition signal filter
14	U400	TDA8759HV/8/C1	Video signal modulus transformer
15	U5	TDA9178T/N1	Video signal picture amendment
16	U600	MT46V2M32LG-4	Frame buffer

ICs FUNCTION INTRODUCTION IN DETAILS

Main Tuner (TAD5-E2122RW2)

Pin	Definition	Description
1	AGC	Auto gain control
2	UT	NC
3	ADD	Ground
4	SCL	IIC bus (Clock)
5	SDA	IIC bus (Data)
6	NC	NC
7	+5V	Power supply
8	NC	NC
9	30V	To produce 0~30V tune voltage
10	NC	NC
11	IF	Intermediate frequency TV signal Intermediate frequency TV signal

Sub Tuner (TMD2-E49IPIWA):

Pin	Definition	Description
1	AGC	Auto gain control
2	NC	NC
3	ADD	Ground
4	SCL	IIC bus (Clock)
5	SDA	IIC bus (Data)
6	NC	NC
7	+5V	Power supply
8	NC	NC
9	33V	To produce 0~30V tune voltage to 0~30V
10	NC	NC
11	IF	Intermediate frequency output (NC)
12	IF	Intermediate frequency output (NC)
13	SW0	Band control
14	SW1	Band control
15	NC	NC
16	SIF	NC
17	AGC	Auto gain control
18	VEDIO	CVBS signal output
19	+5V	Power supply
20	AUDIO	NC

GM1501

GM1501is a kind of processing chassis for dual channels image and video, which is mainly used for LCD displays and integrative TV products. With the resolution of WUXGA, it not only supports PIP technique, but possesses some IC functions applied to image catch, process and clock display. It integrates high velocity AD converter, PLL, high reliability DVI receiver, X86 series mic control and LCDS inverter. See the features as below:

Features

- High quality image zoom function
- Analog RGB signal input interface
- Intelligent output signal auto identification
- Integrated high-power PLL output
- High-reliable self-adaptive DVI input interface
- 4:4:4/4:2:2/CCR656/601 8/16/24bit digital video interface
- Embedded IC for adjustments of gain, contrast, brightness, color saturation, hue and flesh tone.
- Efficiency in reducing EMI electromagnetism inference power consumption
- Inclined grain processing with small angle
- High quality video processing
- Programmable output format
- Embedded LVDS transport
- Advanced OSD
- Embedded micro controller

Pin Description：

Pin	Name	Description
Analog signal input port		
L3	AVSYNC	ADC vertical synchronization signal input
L4	AHSYNC	ADC horizontal synchronization signal input
N2	VGA-SCL	VGA lock input
N1	VGA-SDA	VGA digital input
D1, D2	RED+, RED-	Red analog signal input
C3	SOG	Green synchronization signal
C1, C2	GREEN+, -	Green analog signal input
B1, B2	BLUE+, BLUE-	Blue analog signal input
A2, B3, E3, D3	ADC3.3	ADC3.3Vpower supply
A3, A4	ADC1.8	ADC1.8Vpower supply
A5, B4	ADC-DGND	ADC digital ground
C4, D4, E1, E2, E4	ADC-AGND	ADC analog ground
DVI input port		
N4	DVI-SCL	DDC interface , serial clock signal
N3	DVI-SDA	DDC interface ， serial data signal
A6, B6	RXC+，RXC-	DVI clock input signal
A8～A10 B8～B10	RX0+～RX2+ RX0-～RX2-	DVI input port
B11	REXT	Exterior cut-off resistance
C6～C11	DVI-3.3	DVI 3.3V power supply
D6, D8～D10	DVI-1.8	DVI 1.8V power supply
A7, A11, B5, B7, C7, D7, D11	DVI-GND	DVI ground
Low bandwidth ADC port		
C13	LBADC-33	ADC3.3Vpower supply
A12, B12, C12	LBADC_IN1～ LBADC_IN3	ADC analog input channel
D12	LBADC_RETURN	Channel analog ground
D13	LBADC-GND	Power supply voltage analog ground
OCM bus port		
AA1~AA3, Y1~Y3, W1~W3, V1~V4, U1~U4, T1~T3	OCMADDR0～ OCMADDR19	Address input output port

AB1~AB3, AC1~AC3, AD1~AD4, AE1~AE3, AF1~AF3	OCMDATA0~ OCMDATA15	Data input output port
OCM port control signal		
R1, T4, P1, P2	ROM_CSn~ ROM_CS2n	Part selection signal
R2	OCM_REn	Read enable signal
R3	OCM_WEn	Write enable signal
L1 L2	OCM_INT2 OCM_INT1	Interrupt
M1	OCM_UDO	OCM data output
M2	OCM_UDI	OCM data input
D25	OCM_TIMER1	OCM timer input
Standard definition video control port		
D16	SVCLK	SV pels clock input
C14	SVHSYNC	SV horizontal synchronization signal input
B14	SVVSYNC	SV vertical synchronization signal input
A14	SVODD	Scan status input
A17	SVDV	SV data input
Standard definition video data port		
D14, D15, A15, A16, B15, B16, C15, C16	SVDATA7~ SVDATA0	SV ITU656 data input
Video Control Port		
A20	VCLK	Video pels clock signal
D19	VHS_CSYNC	Video horizontal synchronization signal input
C20	VVS	Video vertical synchronization signal input
B20	VODD	Scan status input
D20	VDV (VSOG)	Video data input
B17	VCLAMP	Video clamp enable output
A21, A22, A23, B21, B22, C21, C22, D21	VGRN7~ VGRN0	Green signal or Y signal input
C17, C18, C19, A18 A19, B18, B19, D18	VRED7~ VRED0	Red signal or V/Cr/Pr signal input
B23, B24, B25, A24 A25, C23, C24, D24	VBLU7~ VBLU0	Blue signal or U/Cb/Pb signal input
Screen Control Port		
A26	PPWR	Screen power control
B26	PBIAS	Screen bias control

D26, C25, C26	PWM2 ~PWM0	Pulse width modulation output
AC7	DCLK	Pels clock output
AC16	OEXTR	Connect external LVDS bias resistance
LVDS Port		
AE14~AE16, AE19~ AE23, AF13~AF16 AF19~AF23, AF11	A0-~A3-, A0+~A3+ B0-~B3-, B0+~B3+	Low voltage difference data input
AD14, AD11, AE13 AE11, AC11, AF10	LVDS_SHIELD [5] ~ LVDS_SHIELD [0]	Low voltage difference protect output
AE12, AF12, AF20, AE20	AC+,AC-,BC+,BC-	Low voltage difference protect input
Screen Port Power Supply		
AD12, AD13, AC12	LVDSB_3.3	LVDS B channel power supply
AC13, AC14, AC15	LVDSB_GND	B channel ground
AC20, AC21, AC22	LVDSA_3.3	LVDS A channel power supply
AD19, AC19, AC20	LVDSA_GND	A channel ground
AE17	VDDD33_LVDS	Analog power supply
AD17	VSSD33_LVDS	Analog ground
Clock Composite and Power Supply		
G4	XTAL	Crystal oscillator interface
F2	VDDD33_PLL，	Digital power supply
H1	VDDD33_SDDS	
J1	VDDD33_DDDS	
G2	VSSD33_PLL	Digital ground
J4	VSSD33_SDDS	
K4	VSSD33_DDDS	
F4	VDDA33_RPLL	Analog power supply
G1	VDDA33_FPLL	
H3	VDDA33_SDDS	
J3	VDDA33_DDDS	
F3	VSSA33_RPLL	Analog ground
H4	VSSA33_FPLL	
H2	VSSA33_DDDS	
J2	VSSA33_DDDS	
G3	TCLK	Reference clock signal input
K2	ACS_RSET_HD	External resistance port

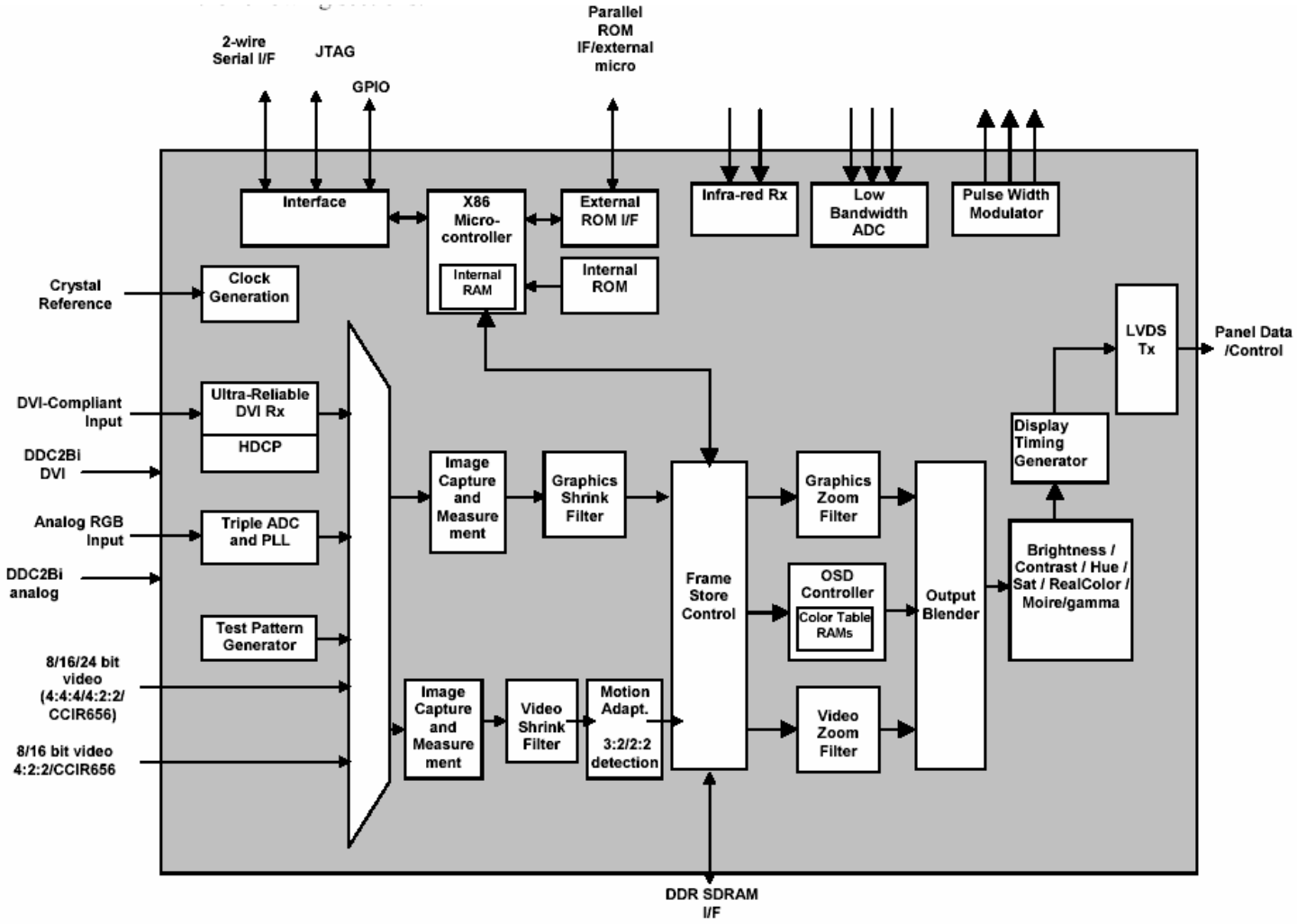
System Signal		
K1	RESETn	Reset signal
M3, M4	IR0，IR1	
P4	MSTR_SCL	Main clock output signal
P3	MSTR_SDA	Main data output/input signal
R4	EXTCLK	External clock input

Frame Memorizer Interface

U24, U23	FSCLKp, FSCLKn	Fine storage clock output
V24, V25	FSRAS, FSCAS	Address output
V26	FSWE	Write enable port
W26	FSCKE	Read enable port
J24	FSVREF	Reference voltage input
K26	FSVREFVSS	Reference voltage ground
W25	FSVREF	Reference voltage input
W24	FSVREFVSS	Reference voltage ground
L26	FSDQS	Data filter
F24~F26, G23~G26 H24~H26, J25, J26, R24~R26, P24~P26 N23~N26,	FSDATA31~ FSDATA0	Data input output port
T24, T25, U25, U26	FSDQM3~ FSDQM0	Data output mark
Y26 Y25	FSBKSEL1，FSBKSEL0	Layer address
AA24~AA26 AB24~AB26, AC24~AC26 AD24~AD26	FSADDR11~ FSADDR0	Range address output
E23, F23, H23, J23, L23, M23, P23, R23, T23, V23, W23, Y23, AA23, AB23, AC23	FS_2.5	2.5V power supply
K23	VDDA18_DLL	1.8V power supply
K25	VSSA18_DLL	Power supply ground
Digital power supply		
K10, K11, K16, K17, L11, L16, T11, T16, T17, U10, U11, U16, U17	CORE_1.8	1.8V power supply

D23, W4, Y4, AA4, AB4, AC4, AC6, D17, D22, AC8, AC10	IO_3.3	3.3V power supply
K12, K13, K14, K15, L10, L12, L13, L14, L15, L17, M10, M11, M12, M13	D_GND	Power ground
A1, AC, D5, AC17, K3, F1	NO_CONNECT	NC

GM1501Internal Block Diagram：

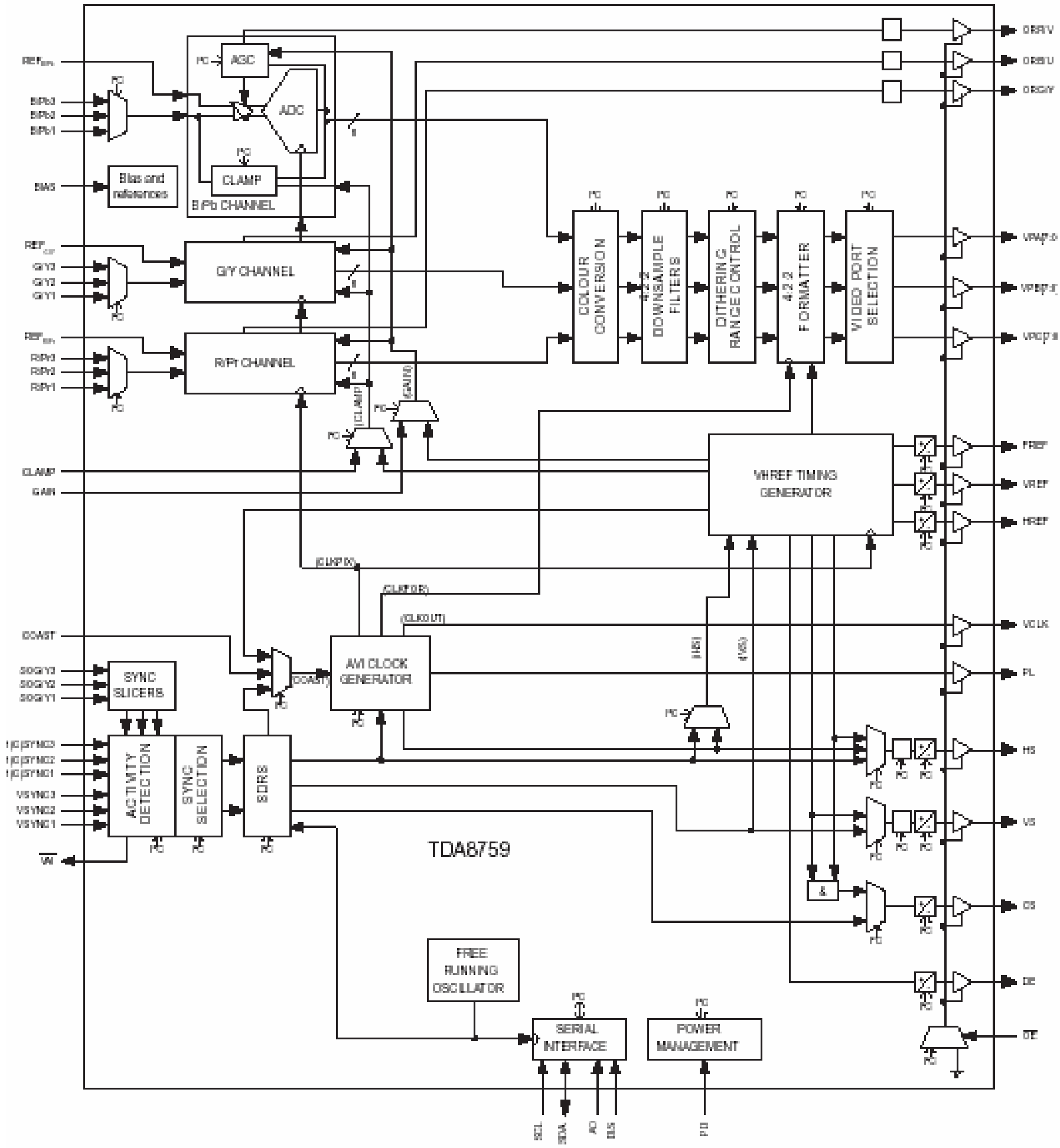


TDA8759:
TDA8759 is a triple 8-bit video converter interface. The IC converts a RGB analog signal into a 24bit RGB or YUV or YCbCr digital signal or converts a YUV or YCbCr analog signal into a YUV or RGB digital signal with a sampling rate up to 81 Msps. The IC supports resolutions from 480i and VGA to HDTV and XGA.

Features

- Triple 8-bit Analog-to-Digital Converter (ADC)
- Three independent analog video sources up to 81 Msps selectable by I2C-bus
- Auto check on interval scan video signal
- 1.8Vand 3.3Vsupplies
- Low gain variation with temperature
- Output format RGB 4:4:4, YUV 4:4:4, YUV 4:2:2, CCIR 656 or YUV 4:2:2 semi-planar standard on output bus
- I²C bus control
- Programmable clock phase adjustment cells
- Amplifier bandwidth of 100 MHz
- Integrated PLL divider
- Power-Down mode

TDA8759 Block Diagram



Pin Description:

Pin	Name	Description
1	HREF	Horizontal reference output
2	VCLK	Video clock output
3, 13, 21, 29, 37, 45, 164	VDDO	Video port output supply voltage
4, 14, 22, 30 38, 46, 165	OGND	Video port output ground
7, 8, 9, 10, 15, 16, 17, 18	VPA0~VPA7	Video port A
11, 116, 130, 132	VDDC	Power supply port
12, 117, 159	CGND	Ground
23~28, 31, 32	VPB0~VPB7	Video port B
35, 36, 39~44	VPC0~VPC7	Video port C
47, 53, 57, 58, 55 60, 66, 70, 71, 75 81, 83, 85, 86,	AGND	Analog ground
48, 54, 59, 61, 67 69, 76, 82, 85, 87, 88	VDDA	Power supply port
49	REFB/Pb	Blue/blue-chrominance channel reference input
52, 51, 50	B/Pb1~ B/Pb3	Blue/blue-chrominance channel analog input
56	BIAS	Bias input
62	REFG/Y	Green/green-chrominance channel reference input
65,64,63	G/Y1~G/Y3	Green/green-chrominance channel analog input
74,73,72	SOG/Y1~SOG/Y3	Sync on green//brightness channel input
77	REFR/Pr	Red/red-chrominance channel reference input
80,79,78	R/Pr1~ R/Pr3	Red/red-chrominance channel analog input
89~92,97~101 112,121,122, 124,125,160~163	TST0~TST17	Reserved for test
93	PD	Power-down control input
94	OE	Output enable input
96	A0	I²C bus address control input
102	COAST	PLL control input
103	GAIN	Gain input
104	CLAMP	Clamp input

105~107	VSYNC1~VSYNC3	Vertical synchronization input
108~110	H(C)SYNC1~ H(C)SYNC3	Horizontal (composite) synchronization input
111	CKEXT	External clock input
113	TCLK	Reserved for test
114	DIS	I²C bus disable control input
118	SDA	I²C bus data input/output
119	SCL	I²C bus clock input
120, 126, 127, 131 133, 142, 148,	IGND	Input digital ground
123, 138, 139, 145 151, 157	VDDI	Input digital supply voltage
166	PL	PLL disable output
167	DE	Data enable output
168	HS	Horizontal synchronization input
169	VS	Vertical synchronization input
170	CS	Color synchronization output
171	ORR/V	Red / chrominance ADCoutput
172	ORB/U	Blue /chrominance ADCoutput
173	ORG/Y	Green / chrominance ADCoutput
174	VAI	Video dynamic indication output
175	FREF	Scan output
17	VREF	Vertical channel reference input

TPA3002D2:

The TPA3002D2 is a 9-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3002D2 can drive stereo speakers as low as 8. The high efficiency of the TPA3002D2 eliminates the need for external heat sinks when playing music.

Features:

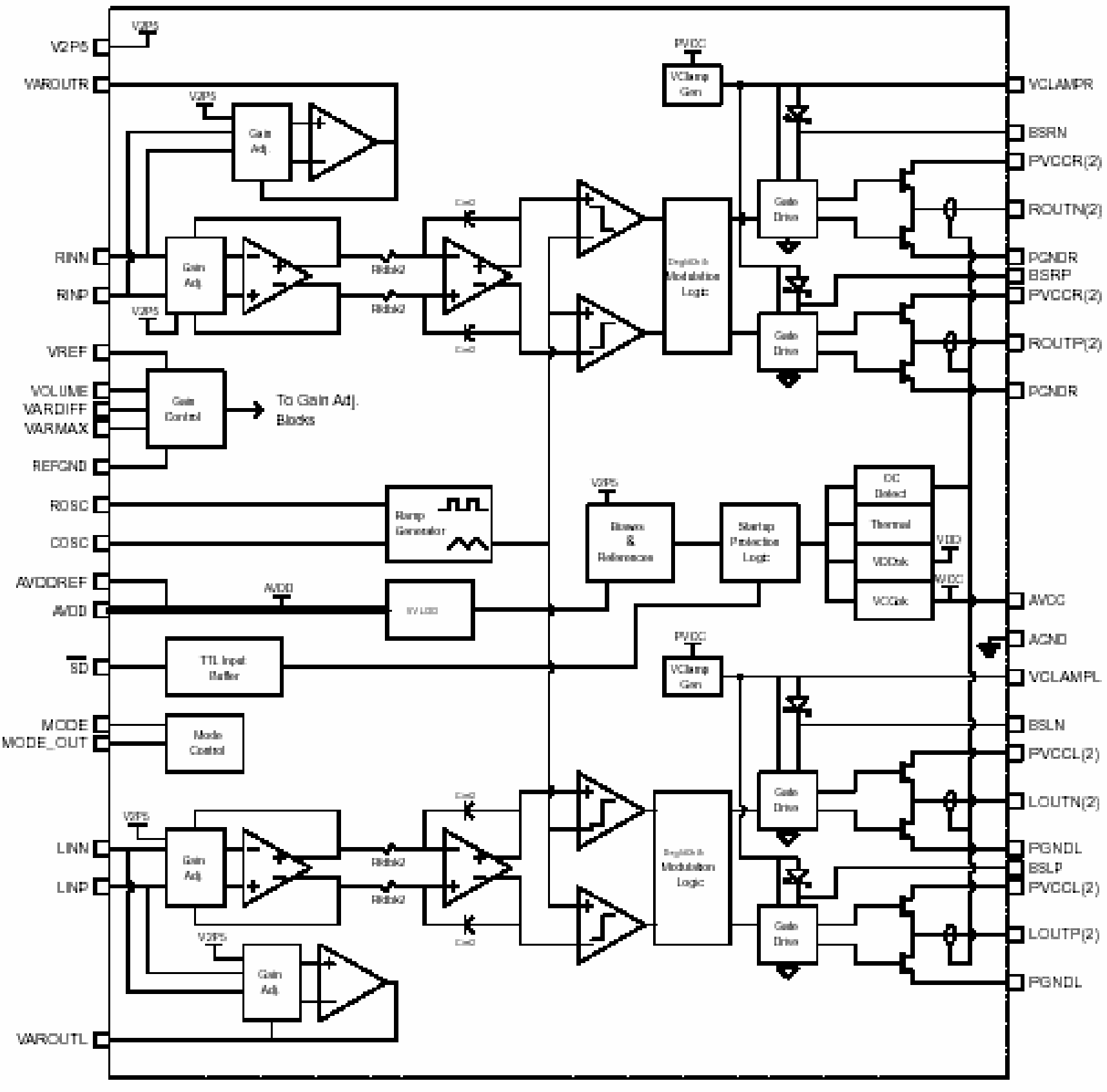
- 9W /Ch into an 8Ω load from 12Vsupply;
- Efficient, class D operation eliminates heat sinks and reduces power supply requirements;
- 32-step DC volume control from -40db~36db;
- Line outputs for external headphone;
- Thermal and short-circuit protection

Pins Functions：

Pin	Name	Description
26, 30	AGND	Analog ground for digital/analog cells in core
33	AVCC	High-voltage analog power supply（8~14V）
29	AVDD	5V regulated output capable of 100mA output
7	AVDDREF	Reference 5V output
13	BSLN	Bootstrap I/O left channel
24	BSLP	
48	BSRN	Bootstrap I/O right channel
37	BSRP	
28	COSC	I/O for charge/discharge currents onto capacitor for ramp generator triangle
6	LINN	Negative differential audio input for left channel
5	LINP	Positive differential audio input for left channel
16，17	LOUTN	Class-D 1/2-H-bridge negative output for left channel
20，21	LOUTP	Class-D 1/2-H-bridge positive output for left channel
34	MODE	Input for MODE control. A logic high on this pin places the amplifier in the variable output mode and the Class-D outputs are disabled. A logic low on this pin places the amplifier in the Class-D mode and Class-D stereo outputs are enabled. Variable outputs (VAROUTL and VAROUTR) are still enabled in Class-D mode to be used as line-level outputs for external amplifiers.
35	MODE_OUT	Output for control of the variable output amplifiers. When the MODE pin (34) is a logic high, the MODE_OUT pin is driven low. When the MODE pin (34) is a logic low, the MODE_OUT pin is driven high. This pin is intended for MUTE control of an external headphone amplifier. Leave unconnected when not used for headphone amplifier control.
18,19,42,43	PGNDR, PGNDL	Power ground for left channel H-bridge Power ground for right channel H-bridge
14,15,22,23	PVCCL	Power supply for left channel H-bridge (tied to pins 22 and 23 internally), not connected to PVCCR or AVCC. PVCCL 22, 23 – Power supply for left channel H-bridge (tied to pins 14 and 15 internally), not connected to PVCCR or AVCC. PVCCR 38,39 – Power supply for right channel H-bridge (tied to pins 46 and 47 internally), not connected to PVCCL or AVCC. PVCCR 46, 47 – Power supply for right channel H-bridge (tied to pins 38 and 39 internally), not connected to PVCCL or AVCC.
38,39,46,47	PVCCR	

12	REFGND	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
32	RINP	Positive differential audio input for right channel
2	RINN	Negative differential audio input for right channel
27	ROSC	Current setting resistor for ramp generator. Nominally equal to 1/8*
44, 45, 40, 41	ROUTN, ROUTP	Class-D 1/2-H-bridge negative output for right channel ROUTP 40, 41 O Class-D 1/2-H-bridge positive output for right channel
1	SD	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to VCC.
9	VARDIFF	DC voltage to set the difference in gain between the Class-D and VAROUT outputs. Connect to GND or AVDDREF if VAROUT outputs are unconnected.
10	VARMAX	DC voltage that sets the maximum gain for the VAROUT outputs. Connect to GND or AVDDREF if VAROUT outputs are unconnected.
31	VAROUTL	Variable output for left channel audio. Line level output for driving external HP amplifier.
32	VAROUTR	VAROUTR 32 O Variable output for right channel audio. Line level output for driving external HP amplifier.
25	VCLAMPL	VCLAMPL 25 – Internally generated voltage supply for left channel bootstrap capacitors.
36	VCLAMPR	Internally generated voltage supply for right channel bootstrap capacitors.
11	VOLUME	DC voltage that sets the gain of the Class-D and VAROUT outputs.
8	VREF	Analog reference for gain control section.
4	V2P5	2.5-V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.

TPA3002D2 External Block Diagram：



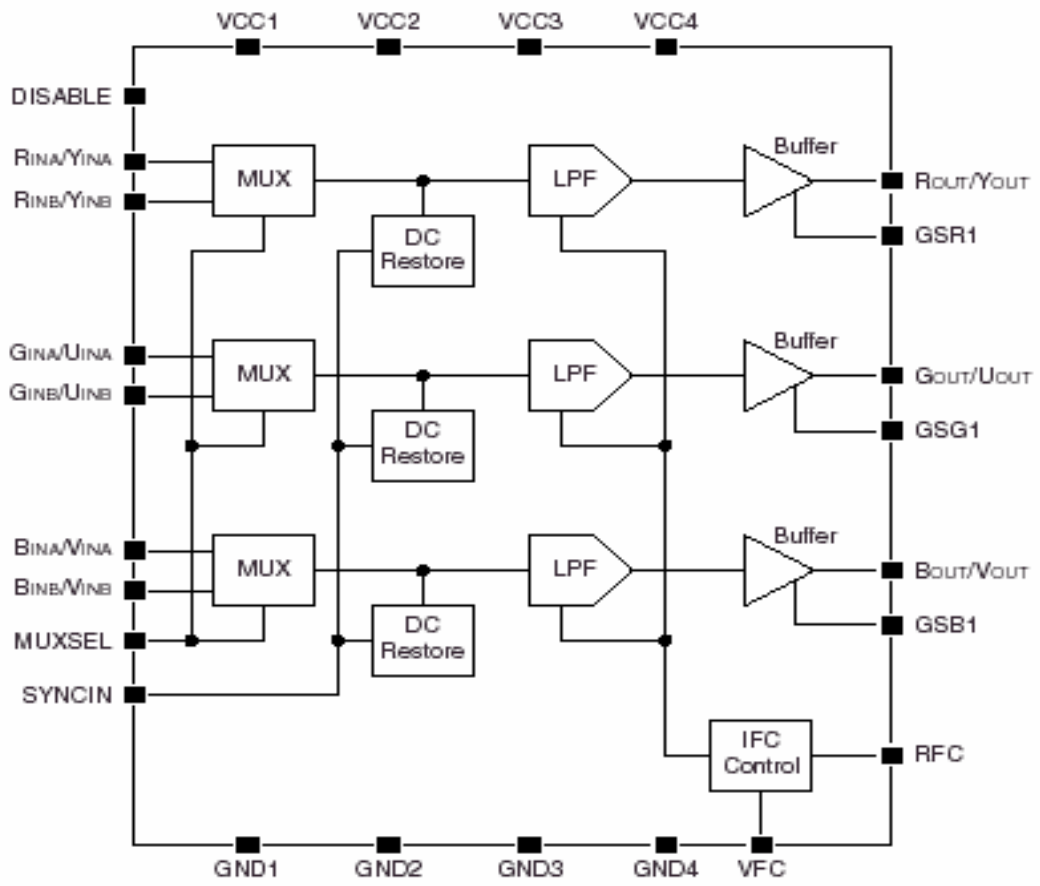
SM5301AS:

Order Butterworth low pass filter configuration. The filter characteristics have been optimized for minimal overshoot and flat group delay, it has a variable cutoff frequency and guaranteed driver-stage channel gain difference and phase difference values.

Features:

- Supply voltage：5V±10%；
- DC voltage level restore sync clamp function
- Output buffer gain switching function: 0, 6dB (input-to-output AC signal gain)
- Channel-to-channel gain difference: 0.5dB(±5% supply voltage variation)
- Channel-to-channel phase difference: 3.5 degree
- Output signal harmonic distortion (all channels): 1.5%
- Cutoff frequency: 5.8 to 37MHz variable

SM5301AS Internal Block Diagram：



Pin Description:

Pin	Name	Description
2	GSG1	GOUT/UOUT output buffer gain set input
1	GINA/UINA	Analog GINA or UINA signal input. Sync signal is input on SYNCIN pin. Analog GINB or UINB signal input. Sync signal is input on SYNCIN pin.
3	GINB/UINB	
5	BINA/VINA	Analog BINA or VINA signal input. Sync signal is input on SYNCIN pin. Analog BINB or VINB signal input. Sync signal is input on SYNCIN pin
7	BINB/VINB	
6	GSB1	BOUT/VOUT output buffer gain set input
9	DISABLE	Power save function. Built-in pull-down resistor.
10, 13, 16, 19	GND	Ground
11	BOUT/VOUT	B/V signal output
14	GOUT/UOUT	Analog 5V supply
17	ROUT/YINB	R/Y signal output
12, 15, 18, 24	VCC	Analog 5V supply
20	RFC	LPF (low pass filter) cutoff frequency setting resistor connection
21	VFC	LPF (low pass filter) cutoff frequency setting voltage input
22	MUXSEL	Input select signal
23	SYNCIN	Filter channel external H-Sync signal input.
26	GSR1	ROUT/YOUT output buffer gain set input
25	RINA/YINA	Analog RINA or YINA signal input. Sync signal is input on SYNCIN pin. Analog RINB or YINB signal input. Sync signal is input on SYNCIN pin.
27	RINB/YINB	
4, 8, 28	NC	No connection (leave open or connect to ground)

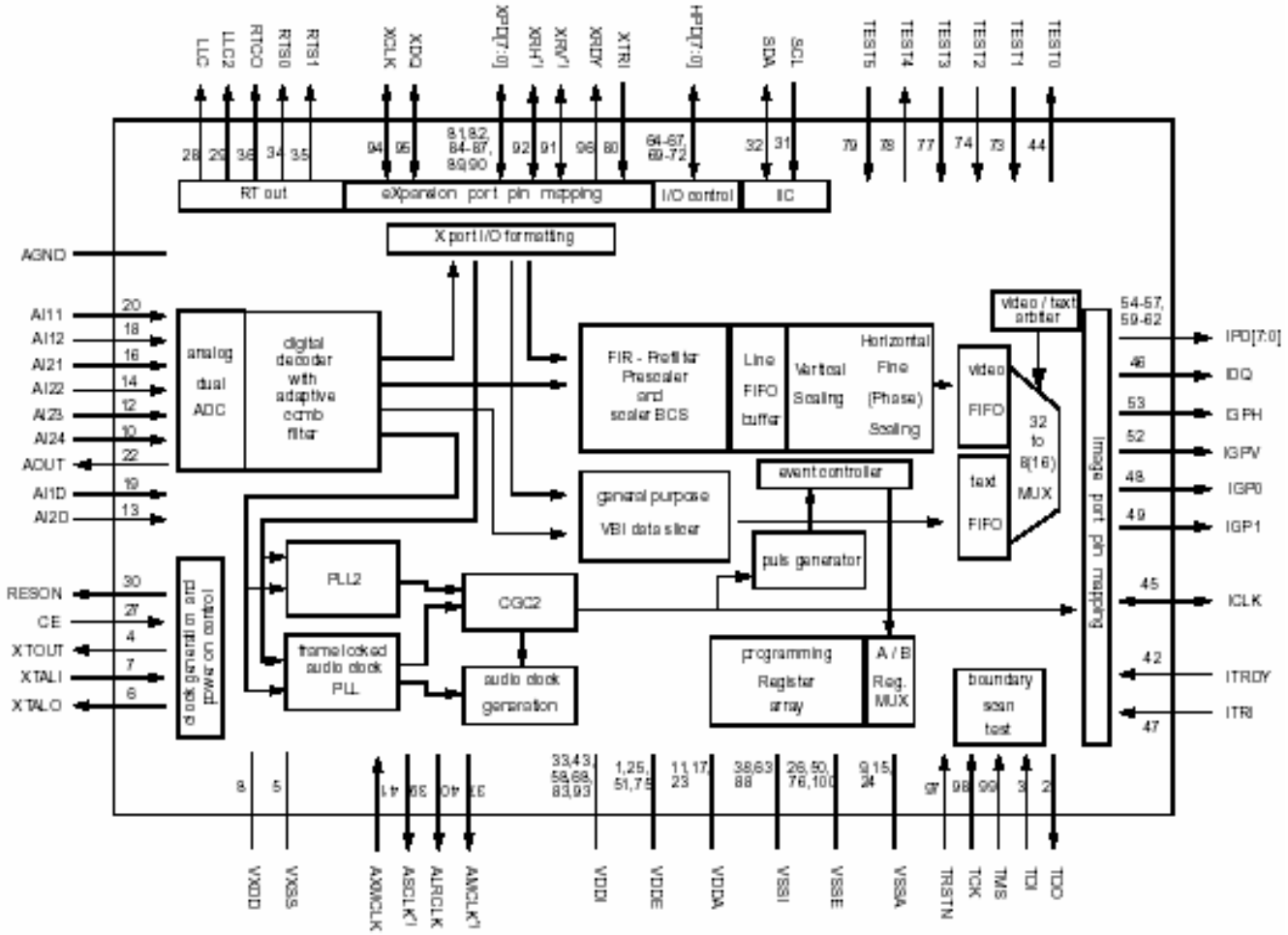
SAA7115:

The SAA7115 is a video capture device for various applications ranging from small screen products like e.g. digital set top boxes, personal video recording applications to big screen devices like e.g. LCD projectors due to it's improved comb filter performance and 10 bit video output capabilities.

Features

- Six analog inputs, internal analog source selectors;
- Two improved 9 Bit CMOS analog-to-digital converter in differential CMOS style;
- Automatic Clamp Control (ACC) for CVBS, Y and C;
- Enhanced Horizontal and vertical Sync Detection;
- . PAL delay line for correcting PAL phase errors;
- Automatic TV/VCR detection; TV/VCR

SAA7115 Internal Diagram:



Pin Function：

Pin	Name	Description
1,8,11,17,23,25,33 43,51,58,68,75,83 93	VDD	Supply voltage port
2	TDO	Test Data Output for Boundary Scan Test (2)
3	TDI	Test Data Input for Boundary Scan Test (with internal pull-up)(2)
4	XTOUT	Crystal oscillator output signal, auxiliary signal
6	XTALO	24.576 (32.11) MHz crystal oscillator output; not connected if XTALI is driven by an external single-ended oscillator. Input terminal for 24.576 (32.11) MHz crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal.
7	XTALI	
6	VXDD	Crystal oscillator power supply
10,12,14,16	AI21~AI24	Analog signal input
13	AI2D	Differential input for ADC channel 2 (pins AI24, AI23, AI22, AI21) differential input for ADC channel 1 (pins AI12, AI11)
19	AI1D	
20	AI11	Analog input 11
18	AI12	Analog input 12
5,9,15,21,24,26,38 50,63,76,88,100	AGND VSS	Ground
22	AOUT	Analog test output (do not connect)
27	CE	Chip Enable or RESET input (with internal pull up)
28	LLC	Line-locked system clock output (27 MHz nominal), for backward compatibility, do not use for new applications line locked clock/2 output (13.5 MHz nominal) for backward compatibility, do not use for new applications
29	LLC2	
30	RESON	RESet Output Not signal
31	SCL	IIC serial clock line (with inactive output path)
32	SDA	IIC serial data line
34	RTS0	Real time status or sync information, controlled by subaddr. “11h and 12h” RTS1 35 O real time status or sync information, controlled by subaddr. “11h and 12h”
35	RTS1	
36	RTCO	Real time control output
37	AMCLK	Audio master clock output
39	ASCLK	Audio serial clock output

40	ALRCLK	Audio lift/right clock output
41	AMXCLK	Audio master external clock input
42	ITRDY	Target ready input, image port (with internal pull up)
45	ICLK	Clock output signal for image-port, LCLK of LPB image port mode, or optional asynchrony backend clock input
46	IDQ	Output data qualifier for image port *(optional: gated clock output)*
47	ITRI	Image-port output control signal, effects all I-port pins incl. ICLK, enable and active polarity is under software control (bits IPE in subaddr. “87”) output path used for **Testing**: scan output
48	IGP0	General purpose output signal 0; image-port (controlled by subaddr. “84”,”85”) General purpose output signal 1; image-port (controlled by subaddr. “84”,”85”), same functions as IGP0
49	IGP1	
52	IGPV	Multi purpose vertical reference output signal; image-port (controlled by subaddr. “84”,”85”)
53	IGPH	Multi purpose horizontal reference output signal; image-port (controlled by subaddr. “84”,”85”)
54~57,59~62	IPD0~IPD7	Image port data output
64~67,69~72	HPD0~HPD7	Host port data I/O, carries UV chrominance information in 16 bit video I/O modes
80	XTRI	X-port output control signal, effects all X-port pins (XPD[7:0], XRH, XRV, XDQ and XCLK) enable and active polarity is under software control (bits XPE in subaddr. “83”)
81,82,84,85, 89,90,86,87	XPD0~XPD7	expansion-port data expansion-port data
91	XRV	vertical reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 0.
92	XRH	horizontal reference I/O expansion-port: In ten bit video output mode: this signal represents the video bit 1.
94	XCLK	clock I/O expansion port
95	XDQ	data qualifier I/O expansion port
96	XRDY	task flag or read signal from scaler, controlled by XRQT (subaddr. 83H)

97	TRSTN	Test ReSeT Not for Boundary Scan Test (with internal pull-up); for board design without Boundary Scan connect TRSTN to 'ground' (1)
98	TCK	Test Clock for Boundary Scan Test (with internal pull-up) (2)
99	TMS	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up) (2)

UOC (TDA15021h):

The UOCIII series combines the functions of a Video Signal Processor (VSP) together with a FLASH embedded TEXT/Control/Graphics □-Controller (TCG □-Controller) and US Closed Caption decoder.

Features

- DVB/VSB IF circuit for preprocessing of digital TV signals;
- Video switch with 3 external CVBS inputs and a CVBS output;
- Automatic Y/C signal detector;
- Adaptive digital (4H/2H) PAL/NTSC comb filter for optimum separation of the luminance and the chrominance signal;
- Picture improvement features with peaking (with switchable center frequency, depeaking, variable positive/negative peak ratio, variable pre-/overshoot ratio and video dependent coring), dynamic skin tone control, gamma control and blue and black stretching. All features are available for CVBS, Y/C and RGB/YPBPR signals.
- The mono intercarrier sound circuit has a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted. In the stereo versions of UOCIII the use of this demodulator is optional for special applications.

  Normally the FM demodulators of the stereo demodulator/decoder part are used (see below).
- The FM-PLL demodulator can be set to centre frequencies of 4.72/5.74 MHz so that a second sound channel can be demodulated. In such an application it is necessary that an external band pass filter is inserted.
- The vision IF and mono intercarrier sound circuit can be used for the demodulation of FM radio signals. With an external FM tuner also signals with an IF frequency of 10.7 MHz can be demodulated. For the QIP90 versions this is valid only for the "stereo" versions
- Built-in adaptable brightness delay circuit
- Switch able brightness signal transmission rate

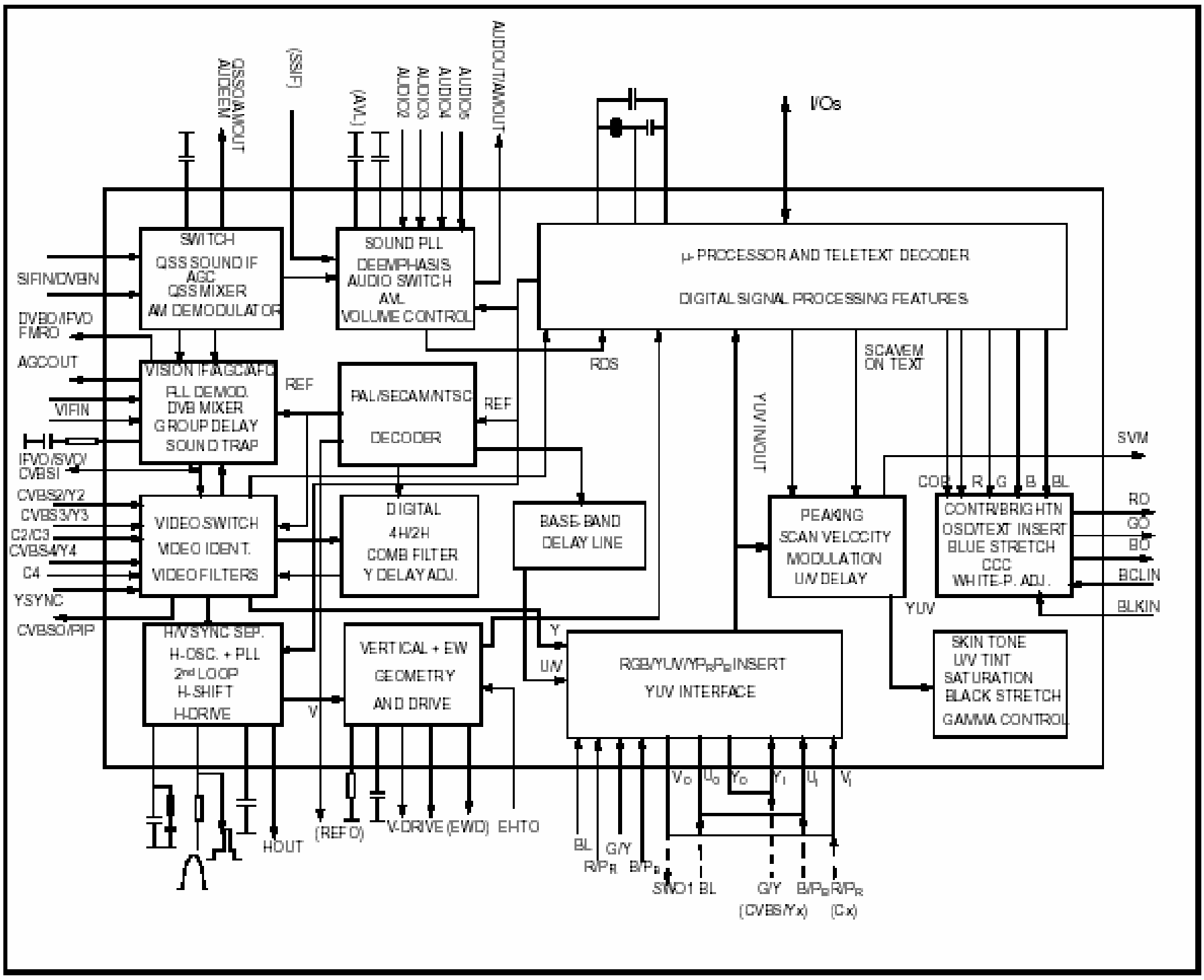
Pin Description：

Pin	Name	Description
1,2,12,18,28,40 68,81,89,92,95,1 01 121,125	VSS, GND	Ground
3,4,45,69,82,88, 90, 91,93,94,96,100, 110,117,118,124	VDD	Power supply
5	VREF_POS_LSL	SDAC input signal
6	VREF_NEG_LSL+HPL	
7	VREF_POS_LSR+HP R	
8	VREF_NEG_HPL+HP R	
9	VREF_POS_HPR	
10	XTALIN	Crystal oscillator input
11	XTALOUT	Crystal oscillator output
13	VGUARD/SWIO	V-guard input / I/O switch
14	DECDIG	decoupling digital supply
15	VP1	decoupling digital supply
16	PH2LF	phase-2 filter
17	PH1LF	phase-1 filter
19	SECPLL	SECAM PLL decoupling
20	DECBG	bandgap decoupling
21	EWD/AVL	East-West drive output or AVL capacitor
22	VDRB	vertical drive B output
23	VDRA	vertical drive A output
24	VIFIN1	IF input 1
25	VIFIN2	IF input 2
27	IREF	reference current input
29	SIFIN1/DVBIN1	SIF input 1 / DVB input 1
30	SIFIN2/DVBIN2	
31	AGCOUT	tuner AGC output
32	EHTO	EHT / overvoltage protection input
33	AVL/SWO/SSIF/REFO /REFIN	Automatic Volume Levelling / switch output reference output / external reference signal DVB operation
34	AUDIOIN5L	audio-5 input (left signal)
35	AUDIOIN5R	audio-5 input (right signal)

Pin	Name	Description
36	AUDOUTSL	audio output for SCART/CINCH (left signal)
37	AUDOUTSR	audio output for SCART/CINCH (right signal) SCART
38	DECSDEM	decoupling sound demodulator
39	QSSO/AMOUT/AUDEEM	QSS intercarrier output / AM output / deemphasis QSS
41	PLLIF	PLL filter
42	SIFAGC/DVBAGC	AGC sound IF / internal-external AGC for DVB applications
43	DVBO/IFVO/FMRO	Digital Video Broadcast output / IF video output
44	DVBO/FMRO	
46	AGC2SIF	AGC capacitor second sound IF
47	VP2	2nd supply voltage TV processor (+5 V)
48	IFVO/SVO/CVBSI	video output / selected CVBS output / CVBS
49	AUDIOIN4L	audio-4 input (left signal)
50	AUDIOIN4R	audio-4 input (right signal)
51	CVBS4/Y4	CVBS/Y input
52	C4	chroma-4 input
53	AUDIOIN2L/SSIF	Audio input
54	AUDIOIN2R	
56	AUDIOIN3L	
57	AUDIOIN3R	
30	AUDOUTLSL	
61	AUDOUTLSR	
62	AUDOUTHPL	
63	AUDOUTHPR	
58	CVBS3/Y3	CVBS/Y input
59	C2/C3	chroma-2/3 input
55	CVBS2/Y2	CVBS/Y input
64	CVBSO/PIP	CVBS/PIP signal output
65	SVM	scan velocity modulation output
66	FBISO/CSY	flyback input/sandcastle output or composite H/V
67	HOUT	horizontal output
70	VIN (R/PRIN2/CX)	V-input for YUV interface
71	UIN (B/PBIN2)	U-input for YUV interface

Pin	Name	Description
72	YIN (G/YIN2/CVBS-YX)	Y-input for YUV interface
73	YSYNC	Y-input for sync separator
74	YOUT	Y-output (for YUV interface)
75	UOUT (INSSW2)	U-output for YUV interface
76	VOUT (SWO1)	V-output for YUV interface
77	INSSW3	3rd RGB / YPBPR insertion input
78	R/PRIN3	3rd R input / PR input
79	G/YIN3	G input / Y input
80	B/PBIN3	3rd B input / PB input
83	BCLIN	Beam current limiter input
85	RO	Red output
86	GO	Green output
87	BO	Blue output
97	INT0/P0.5	External interrupt 0 or port 0.5 (4 mA current sinking direct drive of LEDs)
98,99,102~109 111~116,119,120 122,123,126~ 128	P0.0~ P0.4 P1.0~P1.7,P2.0~P2.5, P3.0~P3.3	Data port

UOC Block Diagram:



The chapter mainly introduces the receipt and dispose of the AV signal, the power supply system and system control process of this TV.

Video Signal Flow:

The IF signal which is demodulated from RF signal by main demodulator is sent through TV board into video decode chassis UOC for decoding, together with the input signals via AV port and two-way SCART ports, then the output analog video signal is sent into analog-to-digital converter TDA8759HV/8/C1 for A/D transform to produce R, G, B digital signals which are transformed in format by GM1601/GM1501, then, it transformed the different input formats into the uniform up-screen signal format. In addition, that TV signal is processed by UOC would produce two-way CVBS signal respectively used for video output of two-way SCART and AV ports.

The signal demodulated from RF signal by sub demodulator is directly sent into submenu video decoder SAA7115HL/V1 for video decoding and A/D conversion, together with the input signals via AV port and two-way SCART ports, then again sent into GM1601/GM1501 to do format transform, the output up-screen is used for submenu display.

The alternative PC, HDTV (YPBPR) and DVI signals are sent directly into GM1601/GM1501 for processing to form uniform up-screen signal.

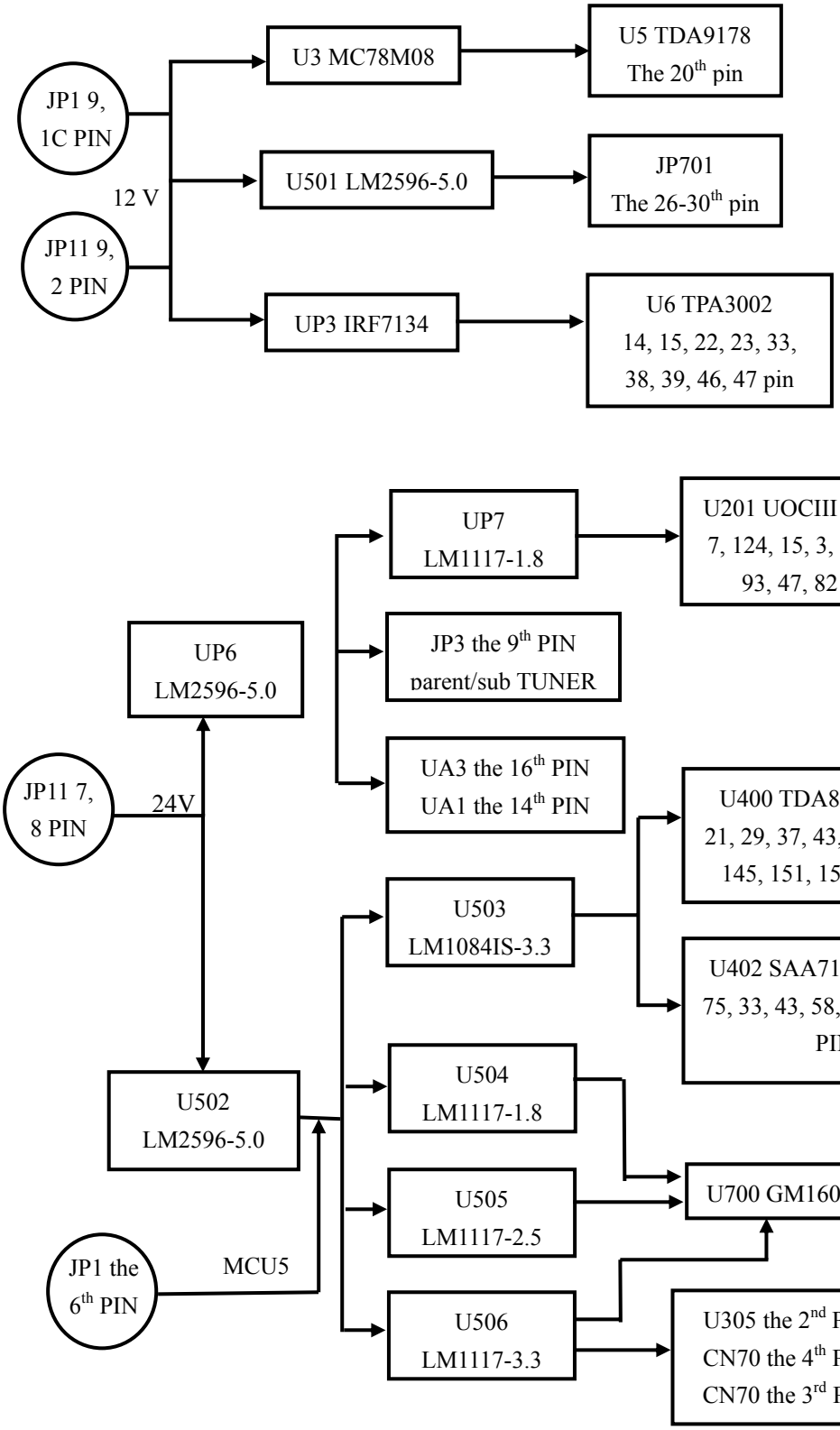
Accompanying Sound Flow:

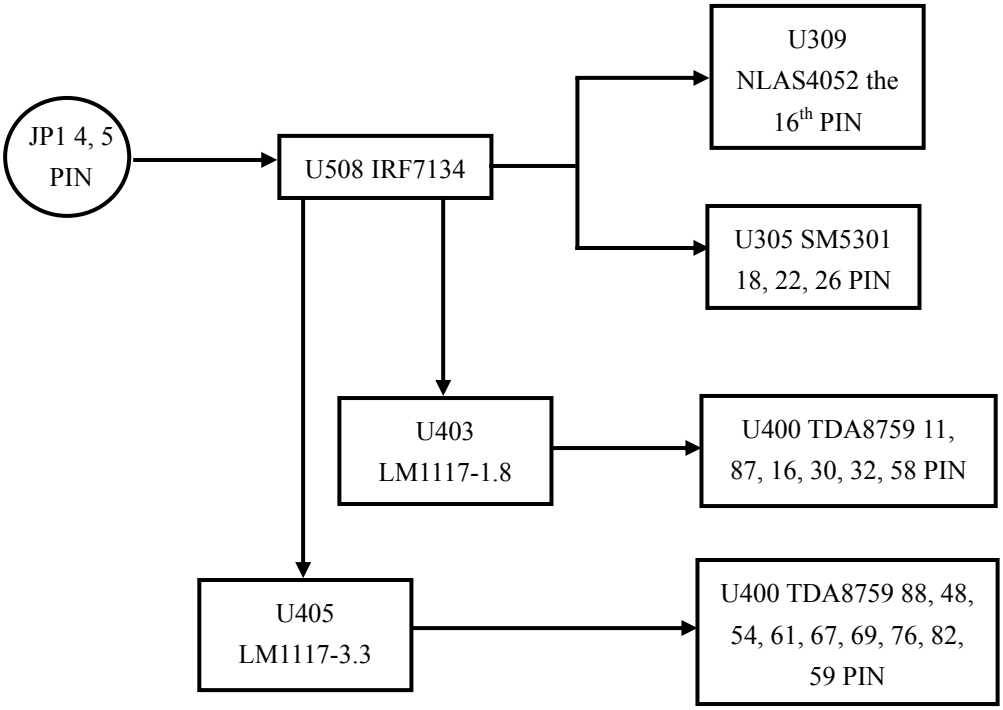
What input sound signal would be sent into UOC for demodulation and sound disposal after selection and simple processing then, the output audio signal is zoomed in by D class TPA3002D2PHPR and is sent into the speaker at last. The other is used for SCART and AV sound output.

TV Power Supply System:

4 channels voltage is transported from the power supply board, they are +24V, +12V, +5V and +5VS. +24V is provided for inverter of LCD panel, +12V is provided for PA, +5V is transformed by the DO (for example: LM1117, LM1084) into 3.3V, 2.5V and 1.8V for IC, it may be turned down under standby mode, while +5VS is provided for MCU, infrared receiver, EEPROM.

5V is divided into two ways, one way is provided for other IC and apparatus, the 5V will be turned down under standby mode, but can not be cut off. The other 5V is provided for MCU, infrared receiver, EEPROM and so on, it would not be cut off under standby mode.

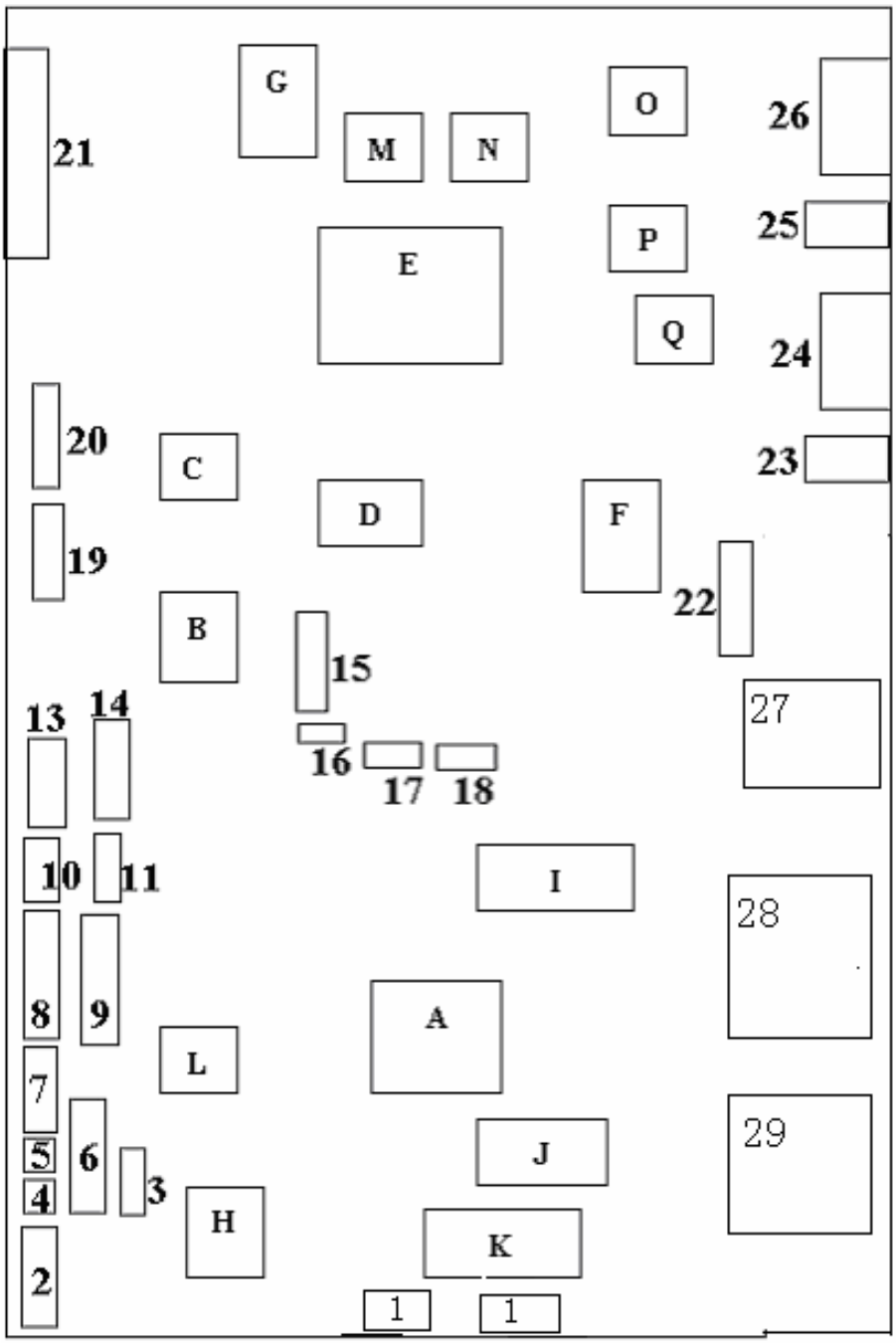

JP1 9, 1C PIN
12 V
JP11 9, 2 PIN
U3 MC78M08
U5 TDA9178 The 20th pin
U501 LM2596-5.0
JP701 The 26-30th pin
UP3 IRF7134
U6 TPA3002 14, 15, 22, 23, 33, 38, 39, 46, 47 pin
UP6 LM2596-5.0
JP11 7, 8 PIN
24V
UP7 LM1117-1.8
U201 UOCIII 100, 11, 7, 124, 15, 3, 118, 96, 93, 47, 82 PIN
JP3 the 9th PIN parent/sub TUNER
UA3 the 16th PIN UA1 the 14th PIN
U400 TDA8759 13, 64, 21, 29, 37, 43, 138, 3, 139, 145, 151, 157, 123 PIN
U503 LM1084IS-3.3
U402 SAA7115 1, 25, 51, 75, 33, 43, 58, 68, 93, 8, 83 PIN
U502 LM2596-5.0
U504 LM1117-1.8
U505 LM1117-2.5
U700 GM1601
JP1 the 6th PIN
MCU5
U506 LM1117-3.3
U305 the 2nd PIN CN70 the 4th PIN CN70 the 3rd PIN



Manostat Pin Voltage in Main Board Schedule

Name	Type	PIN1(V)	PIN2(V)	PIN3(V)	PIN4(V)	PIN5(V)
UP7	LM1117-1.8V	0	1.8	5	1.8	
UP1	LM1117-3.3V	0	3.3	5	3.3	
UP6	LM2596-5.0	24	5	0	5	0
U405	LM1117-3.3	0	3.3	5	3.3	
U3	78M08	12	0	8		
U403	LM1117-1.8V	0	1.8	5	1.8	
U503	LM1806-3.3	0	3.3	5	3.3	
U505	LM1117-2.5	0	2.5	5	2.5	
U506	LM1117-3.3	0	3.3	5	3.3	
U501	LM2596-5.0	12	5	0	5	
U502	LM2596-5.0	24	5	0	5	0
U504	LM1117-1.8V	0	1.8	5	1.8	

Main Components and Socket Locations and Definitions:



Outlet Definition:

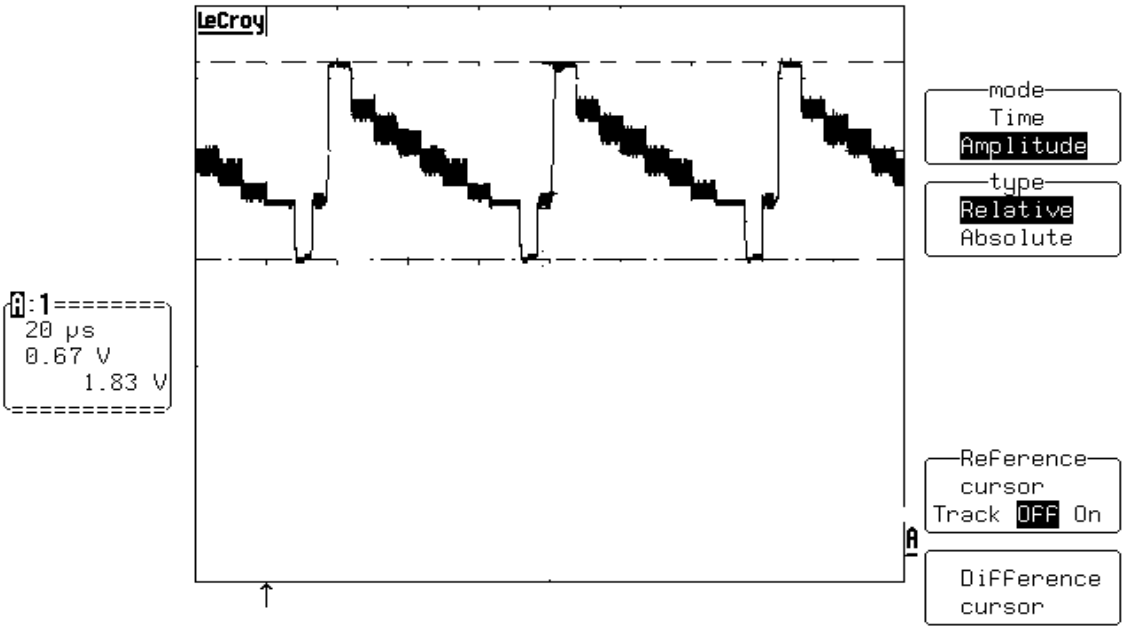
Number	Name	Connected Object	Function Description
1	JP400 JP401	TV board	
2	JP2	Side AV	
3	JP6	DVD AV output	
4	JP7	Speaker	
5	JP8	Speaker	
6	JP4	DVD decode board	
7	JP3	Outside AV input	
8	JP9	Up screen (screen inverter input)	
9	JP10	Up screen (screen inverter input)	
10	JP12	Power supply board	GND, GND, GND, +12V, +12V, +12V
11	J171	Prepare to use	
13	JP11	Power supply board	+12V, +12V, GND, GND, GND, GND, 24V, 24V
14	JP1	Power supply board	SB, GND, GND, 5V, 5V, 5V, GND, GND, 12V, 12V
15	J700	Prepare to use	
16	CN702	Prepare to use	
17	CN700	Remote control	
18	CN701	K board	
19	CN304	Prepare to use	
20	CN303	Prepare to use	
21	JP701	Display	
22	CN306	Prepare to use	
23	AVP303	DVI audio input	
24	CN300	DVI port	
25	AVP300	VG audio input	
26	CN301	VGA port	
27	JPY400 JPY401 JPY402	HDTV AV input	
28	JPA400	SCART (1) interface	
29	JPA401	SCART (2) interface	

Main Components Description:

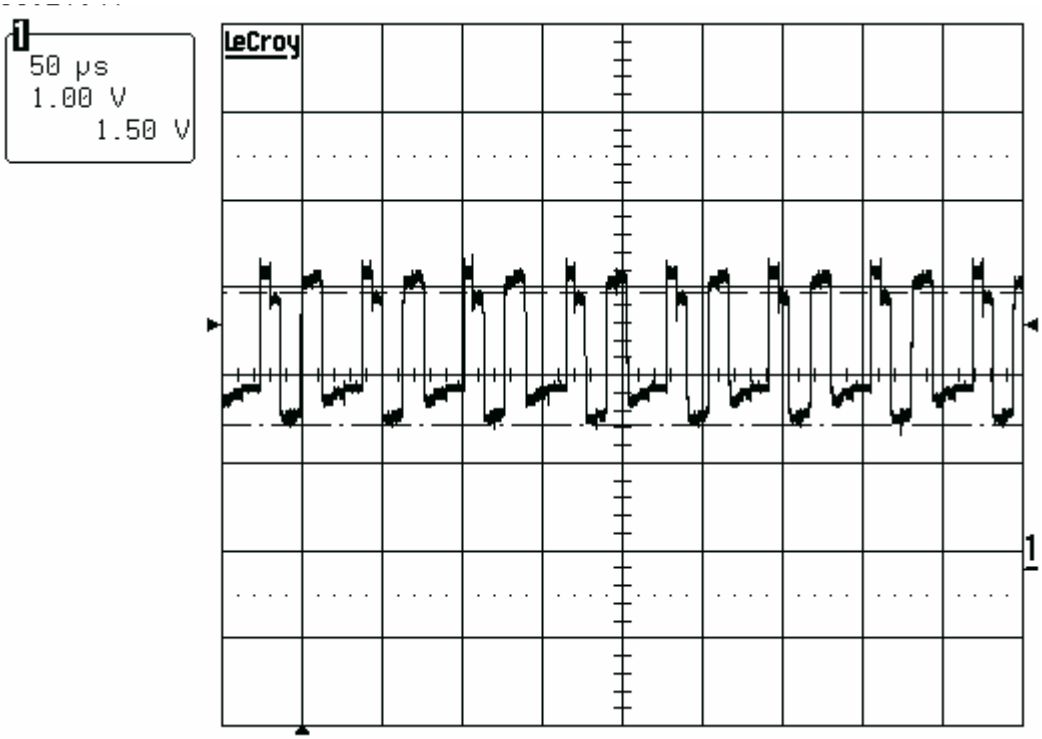
Number	Name	Components	Function Description
A	U201	TDA15021H/N1B07	AV decoder
B	U400	TDA8759HV/8/C1	Video signal AD converter
C	U402	SAA7115HL/V1	Sub channel video decoder
D	U600	MT46V2M32LG-4	Frame buffer memorizer
E	U700	GM1601/GM1501-BD	Video processor
F	U305	SM5302AS-G-ET	HD signal filter
G	U801	AM29LV800DT-70EC	Flash，the TV control procedure put in it
H	U6	TPA3002D2PHPR	Audio PA
I	U5	TDA9178T/N1	Video signal image improve
J	K202	K9656M	Sound surface filter
K	K201	K3953M	Sound surface filter
L	UA3	FSAV330QSCX	Select switch
M	U701	24LC32A T/SN	Buffer
N	U307	FSAV330QSCX	Select switch
O	U306	FSAV330QSCX	Select switch
P	U302	24LC21A T/SN	EEPROM
Q	U303	24LC21A T/SN	EEPROM

Main Points Undulance Illustrations:

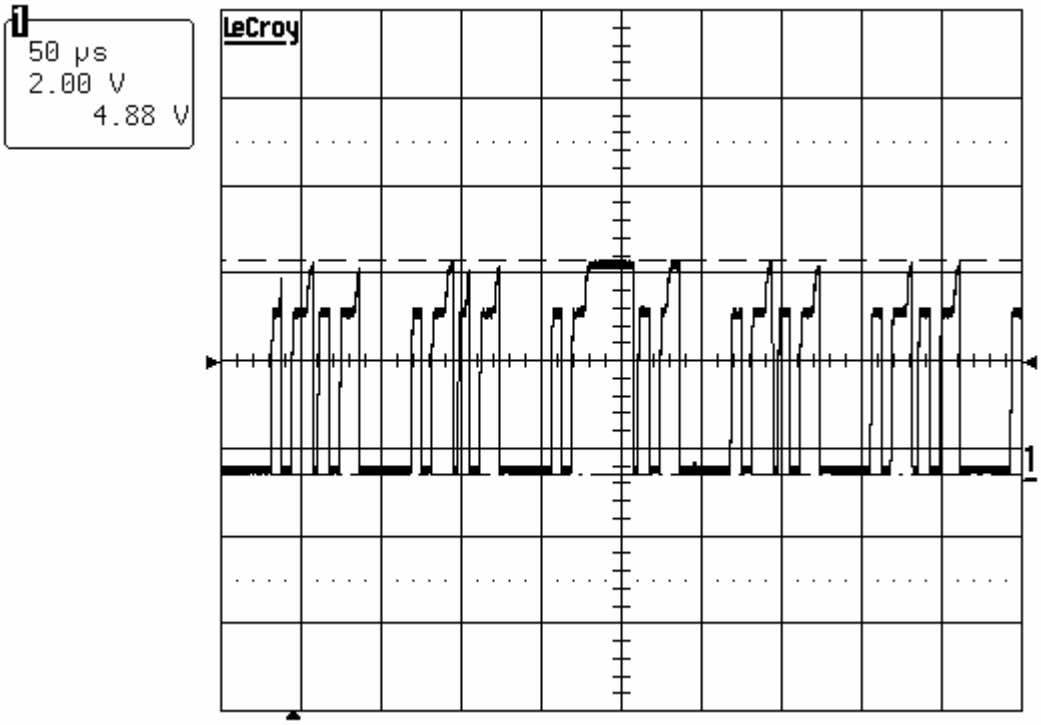
RF input color stripe signal, TV signal undulance in the 19th pin of sub tuner UT1,The undulance of the 10th of SAA7115 also like this:



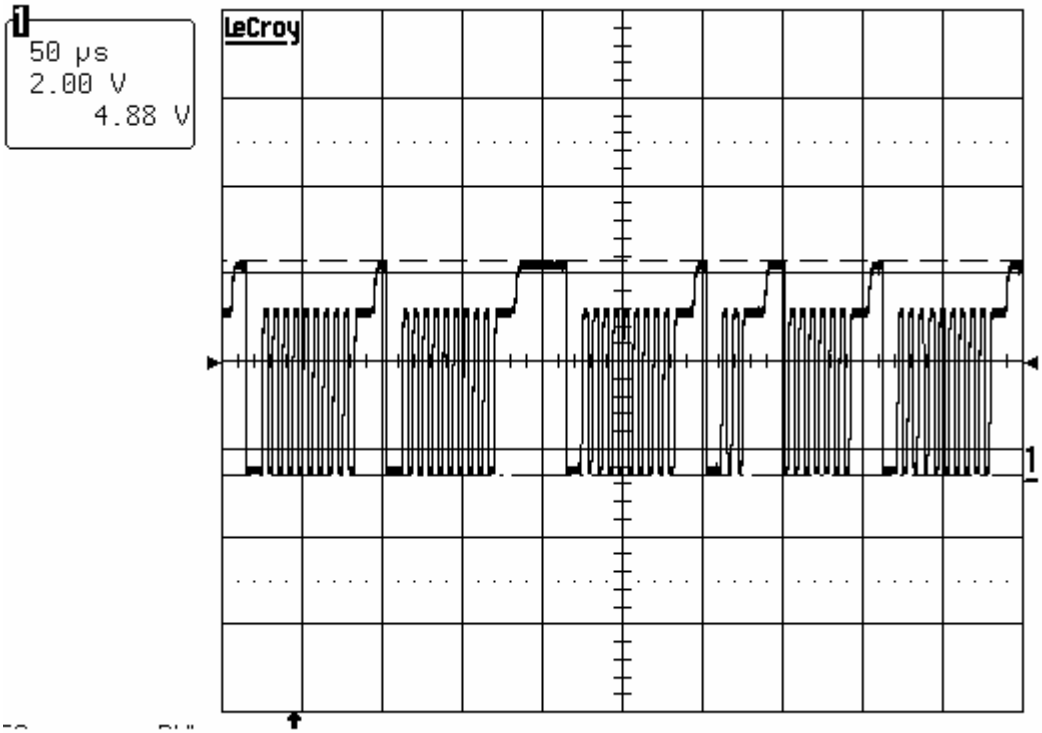
RF input color stripe signal, the Pin85, Pin86, Pin87 of U201 output R,G,B signal undulance, the E pole undulance of Q171,Q172,Q173:



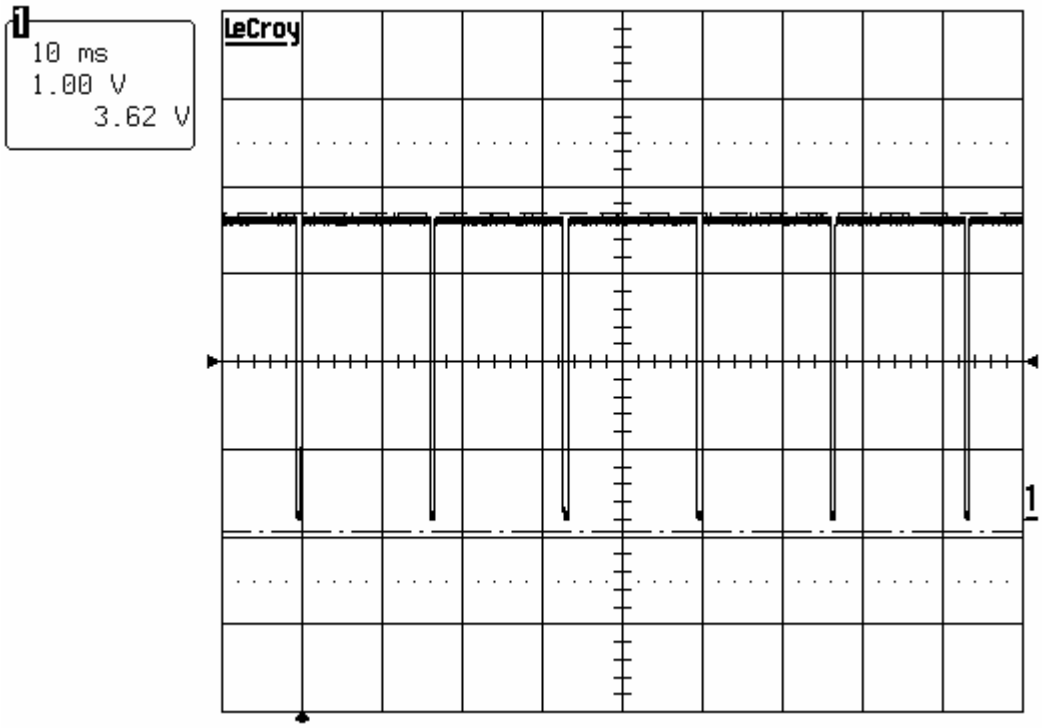
RF input color stripe signal, I²C bus clock signal UOCIII_SCL, the undulance of the 98th pin of U201, the 11th pin of U5, the 4th pin of parent/sub RF tuner:

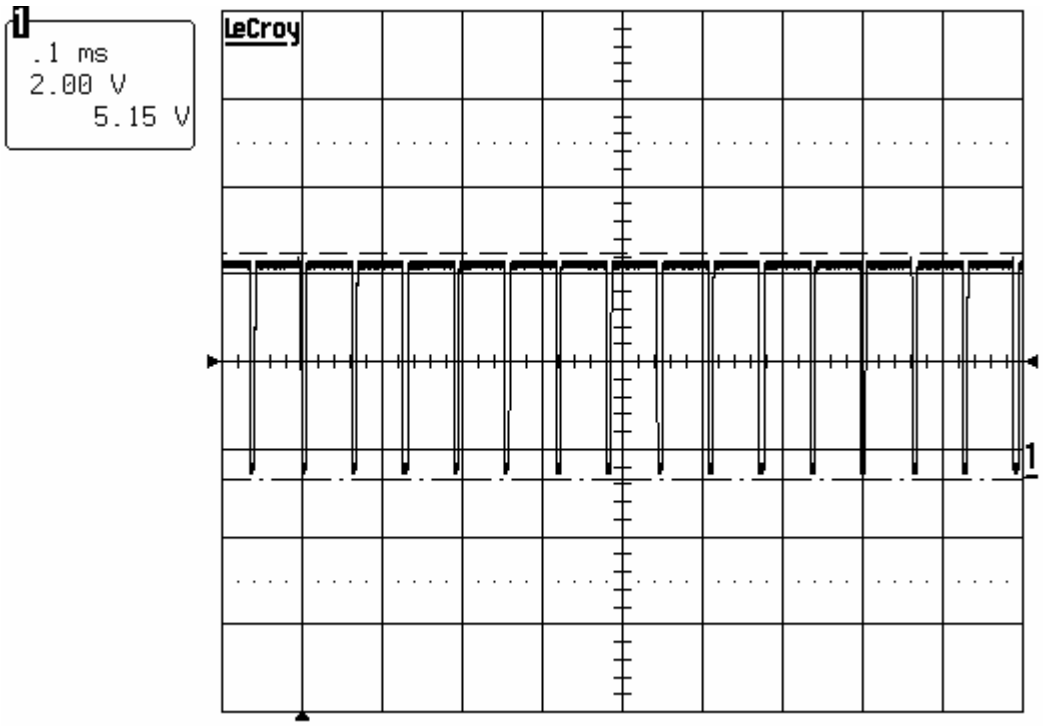


RF input color stripe signal, UOC vertical sync signal, the undulance of the 22th pin of U201, the 105th pin of U400:

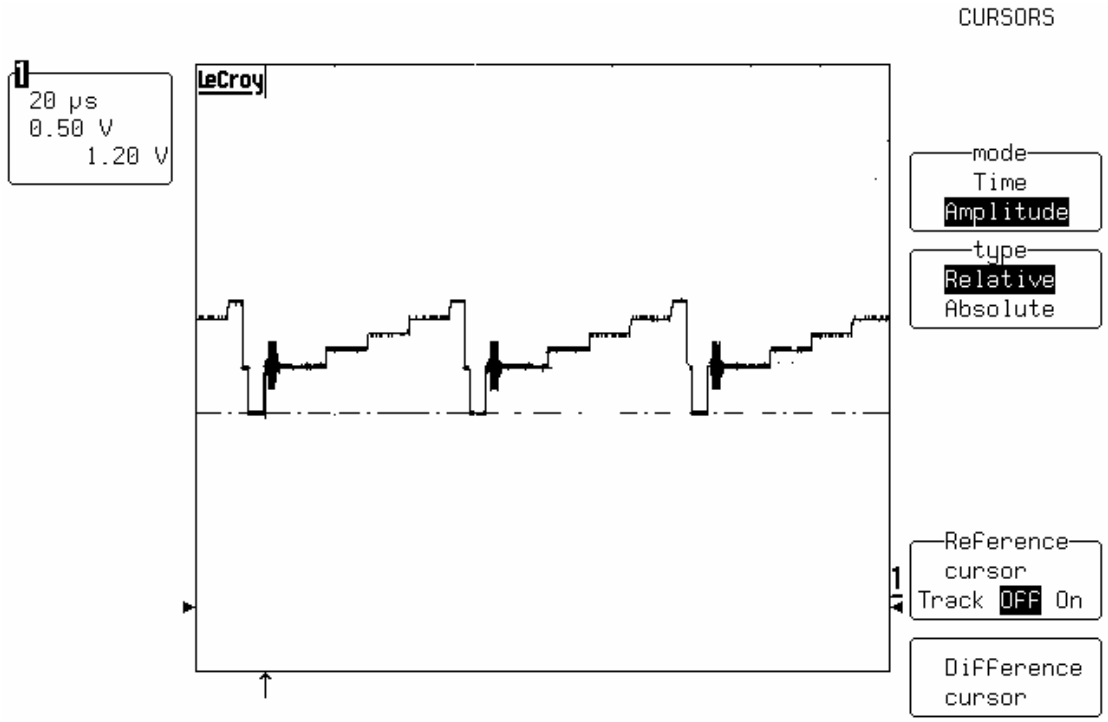


RF input color stripe signal，UOC vertical sync signal , the undulance of the 22th pin of U201,the 105th pin of U400:

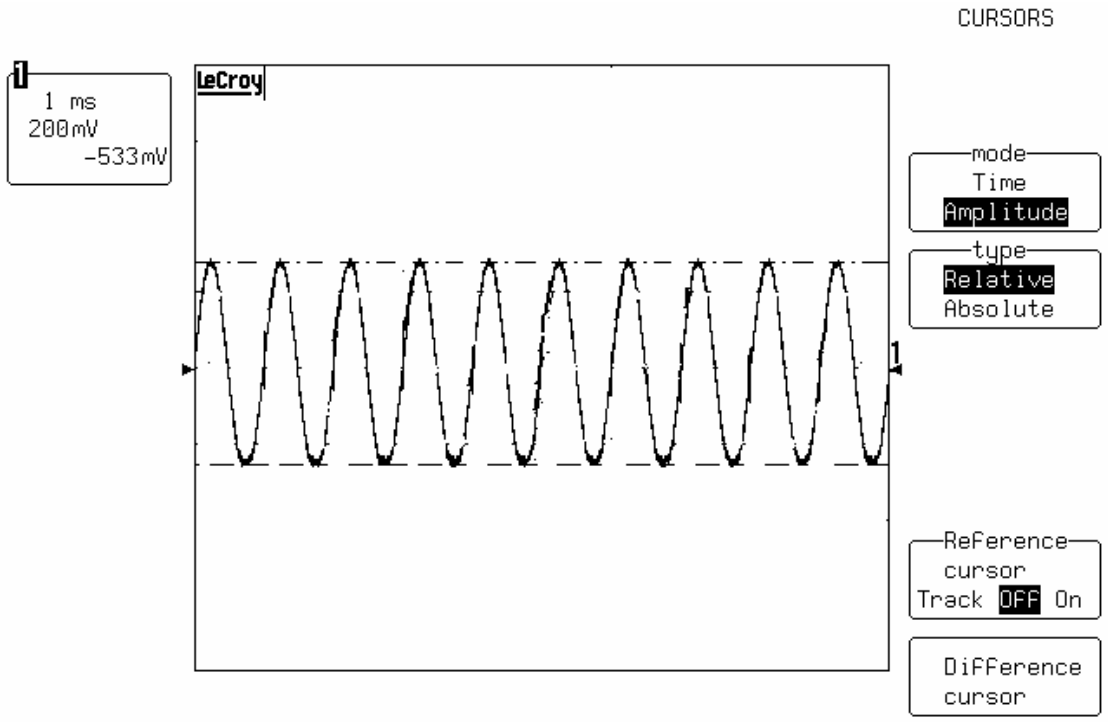




RF input gray ladder signal, the TV signal undulance in the 19th pin of SAA7115:



The 1KHz sound signal input, the undulance of the 60th, 61th pin of U201, the undulance of the 2th, 6th pin of U6 also like this:



The 1KHz sound signal input, the undulance of 16th, 17th, 20th , 2140th , 41th, 44th, 45th pin of U6 and pins:

Location No.	Type	PIN1(V)	PIN2(V)	PIN3(V)	PIN4(V)	PIN5(V)
UP7	LM1117-1.8V	0	1.8	5	1.8	
UP1	LM1117-3.3V	0	3.3	5	3.3	
UP6	LM2596-5.0	24	5	0	5	0
U405	LM1117-3.3	0	3.3	5	3.3	
U3	78M08	12	0	8		
U403	LM1117-1.8V	0	1.8	5	1.8	
U503	LM1806-3.3	0	3.3	5	3.3	
U505	LM1117-2.5	0	2.5	5	2.5	
U506	LM1117-3.3	0	3.3	5	3.3	
U501	LM2596-5.0	12	5	0	5	
U502	LM2596-5.0	24	5	0	5	0
U504	LM1117-1.8V	0	1.8	5	1.8	

SYMPTOMS AND CORRECTION

Symptom	Reason and resolve
The display board of PC no image in DVI.	If some display board of DVI can not receive the data when turning on the TV, there is no output; if pull out the DVI line abruptly, there is also no DVI output; Before starting PC, connect the DVI line with LCD TV steadily. So DVI can receive the correct date from DDC (Display Data Channel) when turning on the TV, DDC is in chassis 24LC21.
No picture but sound, on LOGO when turning on the TV, poor light is bright.	Check the connect line in up screen, and connect the line.
No picture, no sound, no snowflake in TV condition, but AV is normal.	Check the outside of RF (also bus and power supply), there is no problem but no output from RF, so the RF is disabled.
LCD TV can not be controlled (inc red lamp is no but the TV is off, remote control and key press in TV can not control the TV, etc.)	The LCD TV can not work abruptly, power off and turning it on again.

LISTS OF BREAKABLE AND MAINTENANCE PARTS

This list is provided for reference, if change the parameters of those maintain parts of an apparatus, we do not notice in the future. The newest data regard as the correct type or specification.

27″series:

No	Name	Code	Number	PCB Number	Breakable Proportion (%)
1.	Frame	8807400310J	JUJ8.074.031		0.1
2.	Suspend screen	8864000190J	JUJ8.640.019		0.1
3.	Back cover	8807400341J	JUJ8.074.034-1		0.1
4.	Base decorate board	8735600050J	JUJ7.356.005		0.1
5.	Base	8807000130J	JUJ8.070.013		0.1
6.	Main board assembly	8669000353J	JUJ6.690.035-3	PCB JUJ7.820.088	1
7.	AV board assembly	8669300150J	JUJ6.693.015	PCB JUJ7.820.103	0.5
8.	TV board assembly	8669700040J	JUJ6.697.004	PCB JUJ7.820.128	1
9.	Remote receive board assembly	8669400180J	JUJ6.694.018	PCB JUJ7.820.104	0.5
10.	Key press board assembly	8669400190J	JUJ6.694.019	PCB JUJ7.820.091	0.5
11.	Inside power supply module	67128017905	FSP179-4F01		5
12.	LCD display screen	68219602735	V270W1-L04		0.1
13.	Electron tuner	8289100063E	TMI4-C22P2RW		1
14.	Electron tuner	8289100454E	TAD5-C2IP1RW		1
15.	Electric speaker	56224605080	Y2929-01-5W-8Ω		2
16.	Electric speaker	562D6608082	Y50138-01-8W-8Ω		2
17.	Remote controller	8201803760L	KLC5A		1

37″series：

No	Name	Code	Number	PCB Number	Breakable Proportion (%)
1	Frame	8807400430J	JUJ8.074.043		0.1
2	Back cover	8807400442J	JUJ8.074.044-2		0.1
3	Base	8807000160J	JUJ8.070.016		0.1
4	Main board assembly	8669000354J	JUJ6.690.035-9	PCB JUJ7.820.088	1
5	AV board assembly	8669300150J	JUJ6.693.015	PCB JUJ7.820.103	0.5
6	TV board assembly	8669700040J	JUJ6.697.004	PCB JUJ7.820.128	1
7	Remote receive board assembly	8669400200J	JUJ6.694.020	PCB JUJ7.820.104	0.5
8	Key press board assembly	8669400240J	JUJ6.694.024	PCB JUJ7.820.091	0.5
15	Inside power supply module	68213700105	LC370W01		0.1
16	LCD display screen	8864000150J	JUJ8.640.015		0.1
17	Electron tuner	8289100063E	TMI4-C22P2RW		1
18	Electron tuner	8289100454E	TAD5-C2IP1RW		1
19	Electric speaker	56232971081	Y3297-L-10W-8Ω		1
20	Electric speaker	56232971082	Y3297-R-10W-8Ω		1
21	Remote controller	56239390580	Y3939-01-5W-8Ω		2
22	Remote emitter	8201803510L	KLC5B		1

FACTORY MODE AND NOTICE

Enter into factory menu

Enter into child lock of main menu in TV mode, press “OK”, the password input box will appear;

USE remote control to input the follows in order: 7, red key, 9, blue key, then you can enter into factory mode menu. After entering into factory mode menu, sign of the factory menu M will appear.

Factory menu and setup

Factory menu display is below:

M

Index: 1

HWUC_BRI 0x1F

The ***M*** denotes entering into factory mode now, the figures of index denotes the index number now, the HWUC_BRI denotes the name of adjusting item now, the 0X1F denotes the numerical value.

Each adjusting item have only one index number, the operator press the numeric key or press P+/P- directly.

Optional and adjustable items, the corresponding relation of index number and adjusting item is below:

(Index)	Name	Definition	Operating key	Remark
1	HWUC_BRI	UOCIII subsidiary brightness	V+/V-	Tune subsidiary brightness
2	HWUC_SAT	UOCIII saturation	V+/V-	Tune subsidiary saturation
3	HWUC_CON	UOCIII contrast	V+/V-	Tune subsidiary contrast
4	HWUC_AGC	UOCIII AGC	V+/V-	Tune AGC
5	PIP Brightness	7115 subsidiary brightness	V+/V-	Open sub picture When tuning it
6	PIP VGA Contrast	7115 contrast	V+/V-	Open sub picture When tuning it
7	Balance	Sound balance	V+/V-	The tuning value is 50, -50, 0
8	Volume	Sound Volume	V+/V-	Step is 10
9	Sound System	Sound System	V+/V-	DK/I/BG/M
10	Auto Search	Auto searching	V+/ok	Source of Signal is TV
11	White Balance	White balance	V+/ok	
12	Auto Color	Auto color revise	V+/ok	Source of Signal VGA /YPbPr /TV
13	DVD	DVD preset	V+/V-	1 represent preset
14	BBE	BBE preset	V+/V-	1 represent preset
15	TruSurround	TruSurround preset	V+/V-	1 represent preset
16	SALESFOR	SALESFOR	V+/V-	Set sell country
17	Factory Out	initialization	V+/ok	Leave factory set
18	ClearEEProm	initialize EEPRom	V+/ok	Initialize the storage date
19	D Mode	Enter into design mode	V+/ok	Adjustable design mode all the parameter
20	DPF	DPF preset	V+/V-	1represent preset
21	BBE_CONT	BBE plus set	V+/V-	Tune BBE plus
22	BBE_PROC	BBE plus set	V+/V-	Tune BBE plus
23	Newcom	Newcom set	V+/V-	1represent preset

Notice:

1. If no especial demand, please do not enter into the 20th item (design mode).
2. When tuning the 16th item, the storage data will be cleaned off. Therefore, if not necessary, please do not adjust it, the items of index number 1, 2, 3, 4, 5, 6 are not necessary to adjust.

Methods of adjustment for factory menu

1. Select the adjusting item operator can skip to the adjusting items by pressing the number key, also can select the adjusting item in the order of P+/P-.when pressing the number key. If the adjusting item is 1~9,input the corresponding number keys and press down “OK”. If the adjusting items tens digit, input a tens digit for example, press number key 8 when adjusting the volume, you can see the color which become green, then press down “OK”. The color of index number turns red, so you already selected corresponding volume adjusting item.
2. Adjusting methods adjust it according to the operating key in above list. For one acting operation. Press OK/V+ example AutoColor. For some variable add/reduce, example Volume, press V+/V-.
   All menu functions are on in factory mode, if necessary you can use menu to check the items and effect test.

Factory debug item

1. Auto color revise (AutoColor)
   You should finish auto color revise first before factory debug. Revise in TV, YPBPR and PC respectively.
   - Requisite Meters
     PC one
     HD signal source one
   - Debug (Revise in TV, YPBPR and PC respectively)
     Park the channel in C-3 under TV mode, then do AutoColor.
     Input color stripe signal in YPbPr and do AutoColor.
     Input window signal in PC, the window is white with black signal around.
     The result will appear on screen after AutoColor adjustment. As for TV, you should make the adjustment results of Rgain, Ggain and Bgain close to 0×80; If the difference is too great, adjust the value of HWUC_CON(auxiliary saturation),and readjust the AutoColor.
2. White balance, color temperature adjustment
   - Requisite Meters
     CHROMA 7120 color analyze instrument (or same function instrument, contain color coordinate – chroma diversion card) one
     White balance adjusting frock（request the video output range 0-1V is adjustable, 750hm load) one
   - Preparation
     a. Connect all equipment, switch the condition of LCD TV to AV.
     b. Set the picture of LCD TV for standard condition
     Set the distance of light receiver of white balance from center place of LCD display screen for 15cm±3cm.
     Make sure that the environmental brightness is below 2cd/m2.

- White balance, color temperature adjustment

  Before adjusting it, put the first LCD TV in AV condition, and the image in standard condition, white balance adjust frock send the white vertical signal output from video into AV, adjust output range of balance adjust frock, make the brightness of the LCD TV 200±20cd/m2 (use CHROMA 7120 color analyze instrument to obtain the brightness), then fix the video output range of white balance adjust frock (until all the LCD TV are adjusted).

  Enter into white balance adjusting item of factory mode, change R, G, B value (try best to adjust this 3 value to maximum).

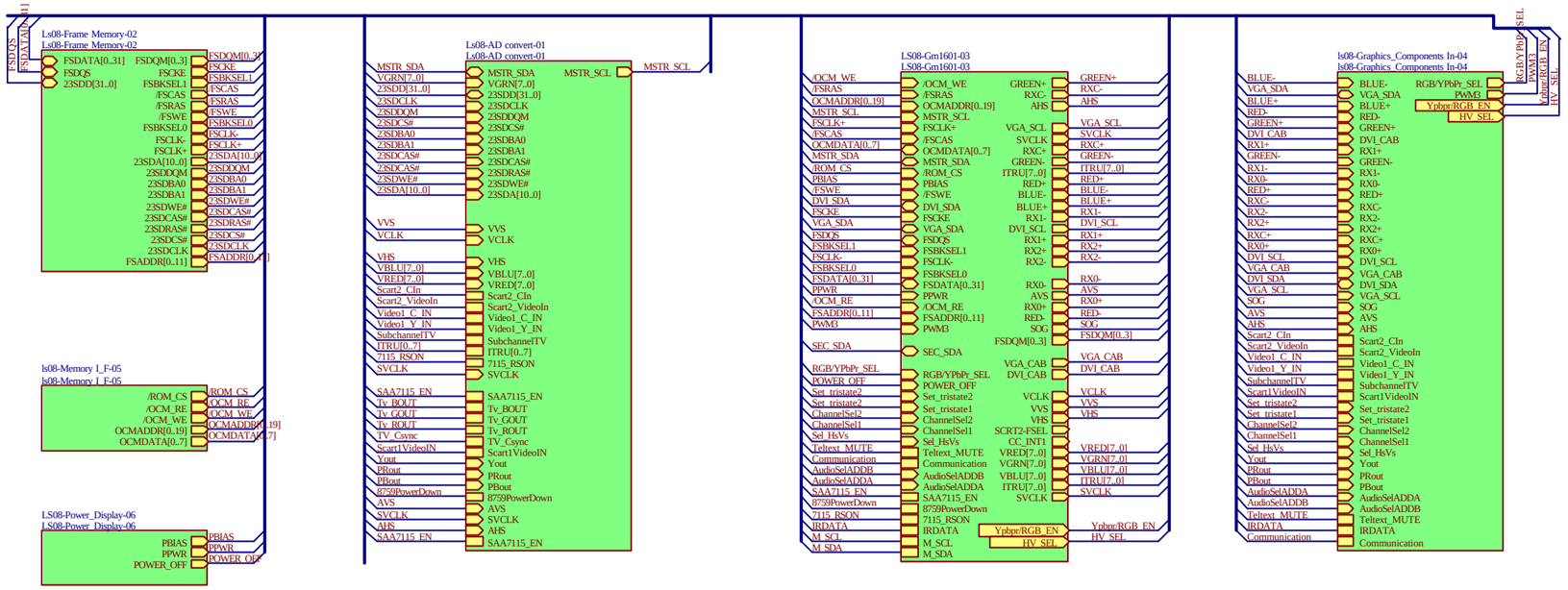
  Make color temperature coordinates value same to this table below: (Error limitation ± 4%):

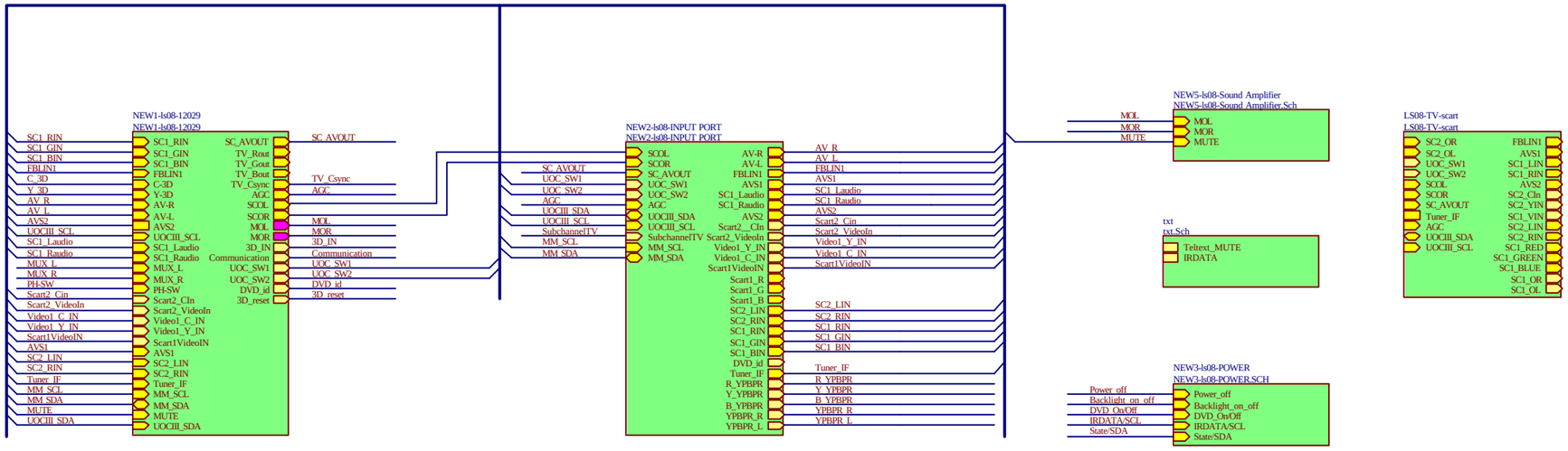
	X	Y
K12000	0.270	0.277

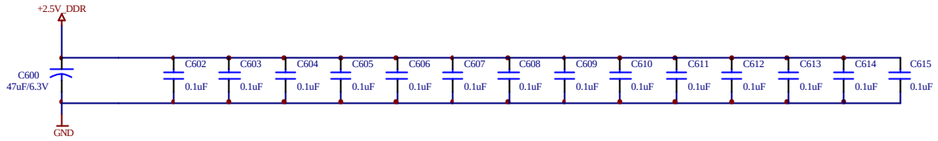
Note:

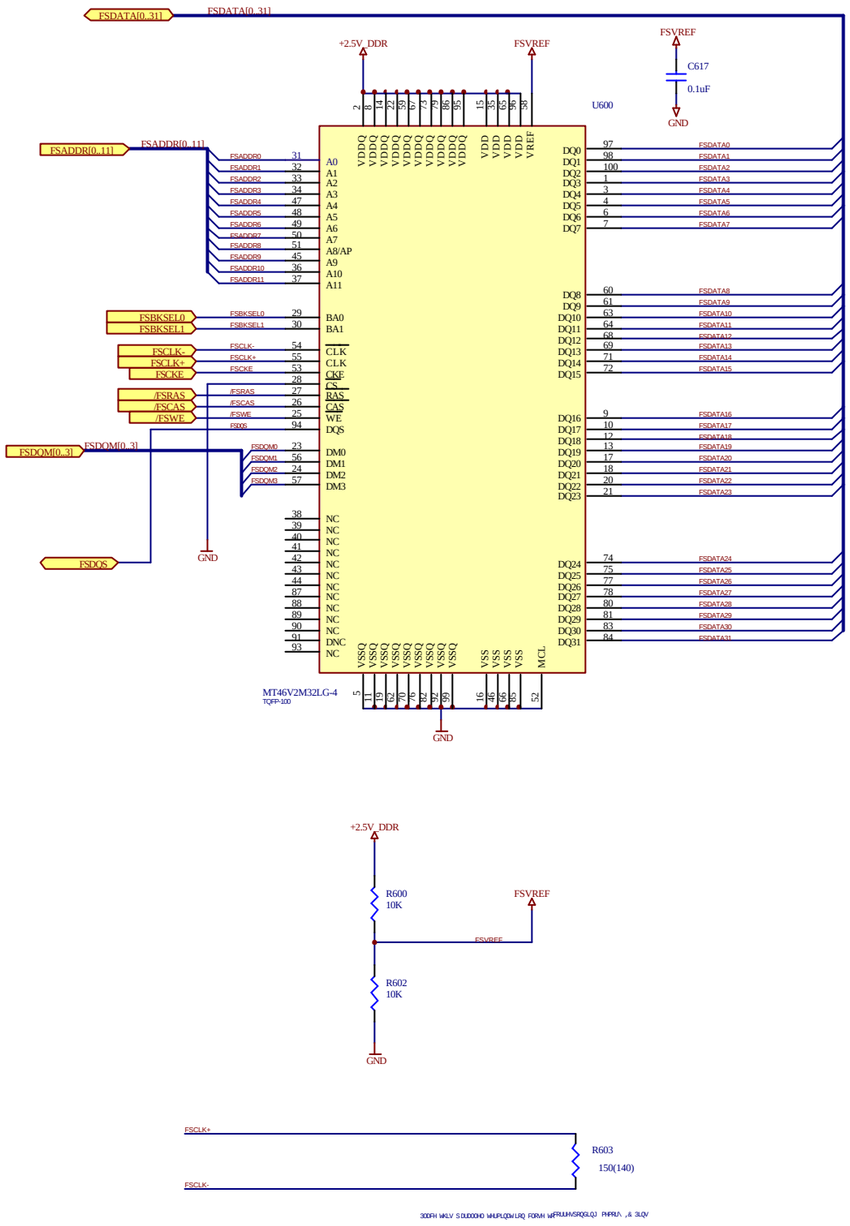
After color temperature and color coordinates meet the above requirements, you should judge whether is any abnormal color or not, that is to say, is the value of Δuv 0, if not, it means abnormal color, then you should adjust values of R, G, B to 0, meanwhile, meet the color coordinates requirements.

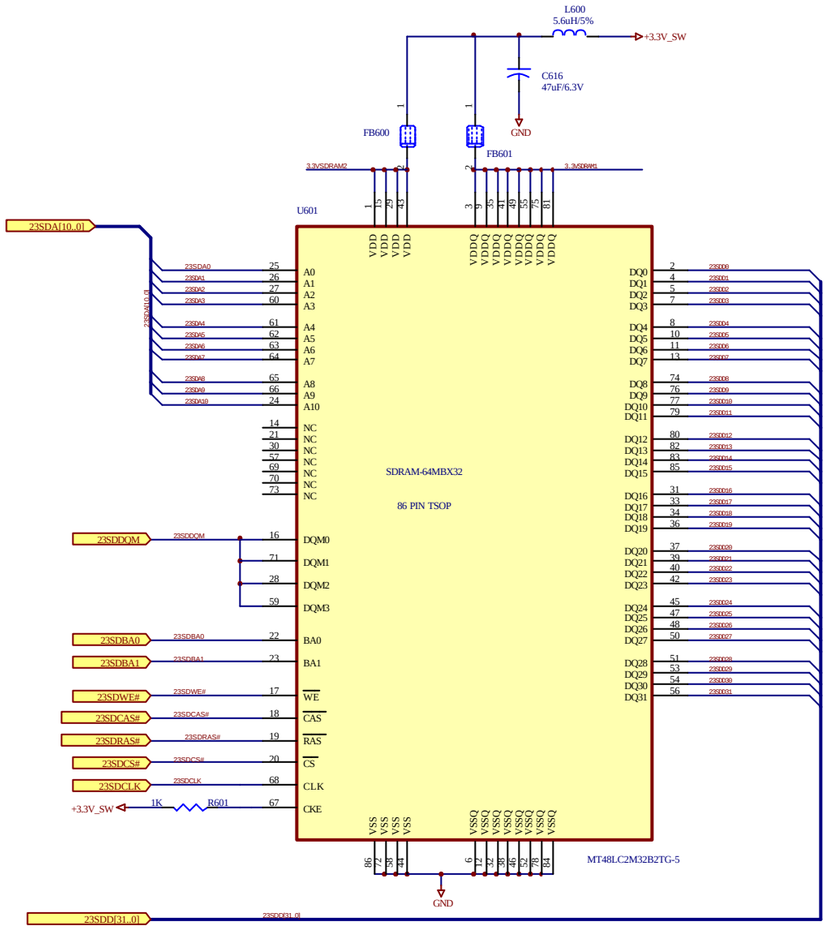
CIRCUIT DIAGRAM





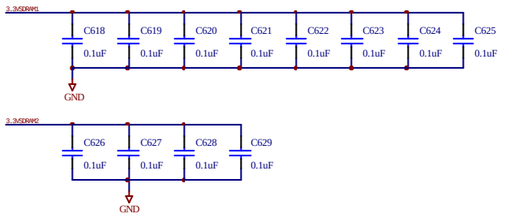

+2.5V_DDR
C600
47uF/6.3V
GND
C602
C603
C604
C605
C606
C607
C608
C609
C610
C611
C612
C613
C614
C615
0.1uF

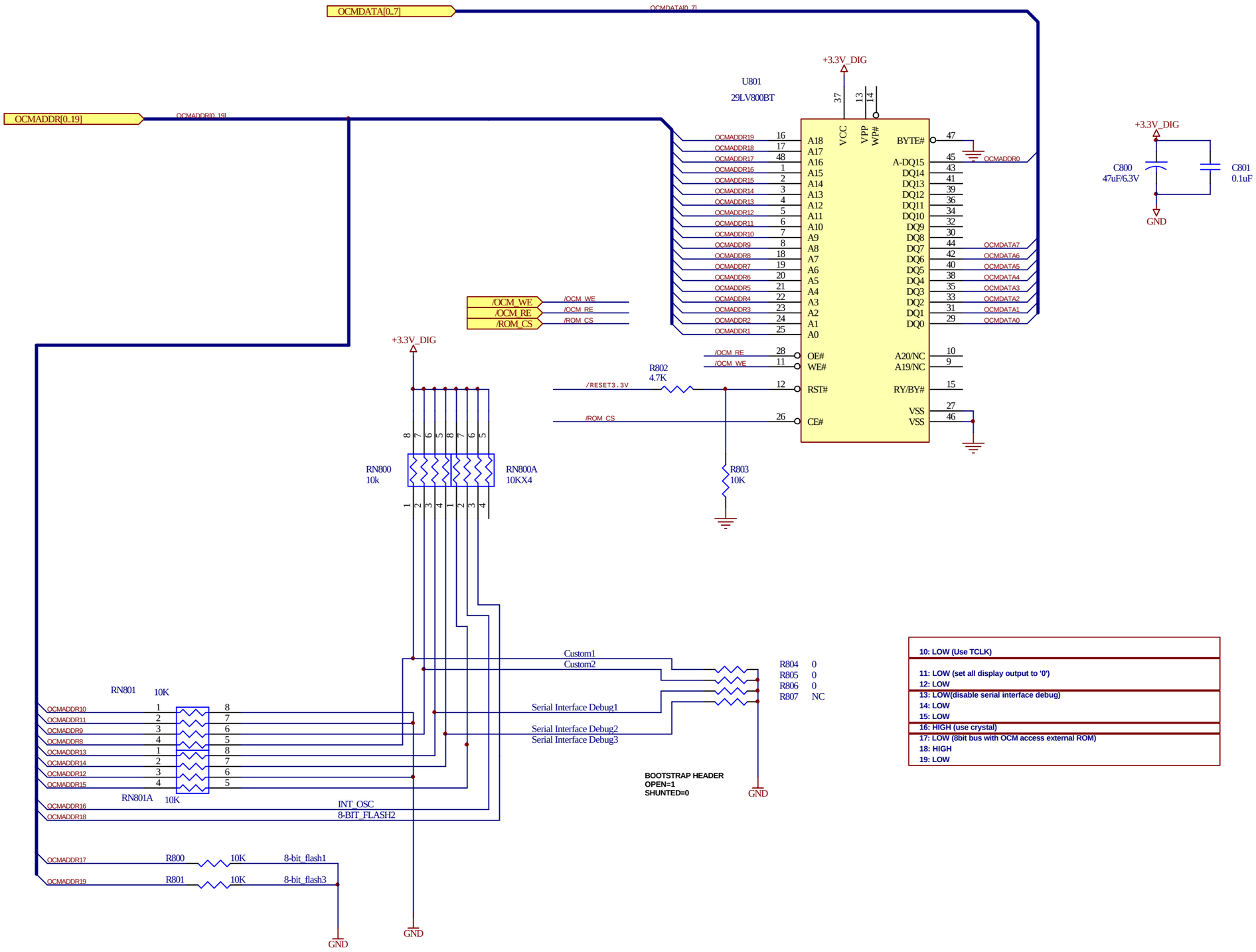

FSDATA[0..31]
FSADDR[0..11]
FSDQM[0..3]
FSDQS
+2.5V_DDR
FSVREF
C617
0.1uF
GND
U600
A0
A1
A2
A3
A4
A5
A6
A7
A8/AP
A9
A10
A11
BA0
BA1
CLK
CKE
CS
RAS
CAS
WE
DQS
DM0
DM1
DM2
DM3
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
NC
DNC
VDD
VDDQ
VSS
VSSQ
MCL
VREF
MT46V2M32LG-4
TQFP-100

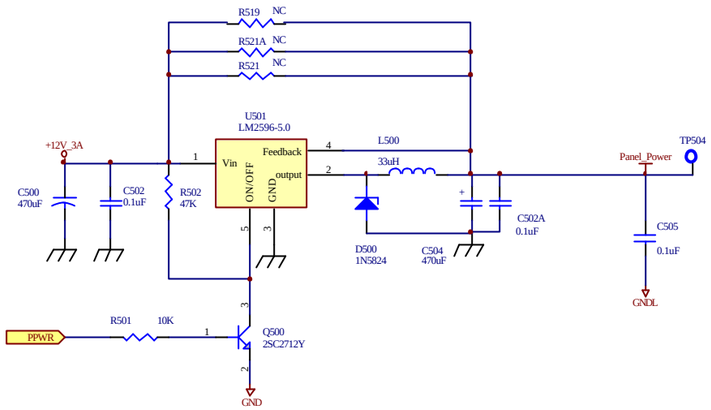

L600
5.6uH/5%
+3.3V_SW
C616
47uF/6.3V
GND
FB600
FB601
3.3VSDRAM2
3.3VSDRAM1
U601
23SDA[10..0]
23SDD[31..0]
23SDDQM
23SDBA0
23SDBA1
23SDWE#
23SDCAS#
23SDRAS#
23SDCS#
23SDCLK
+3.3V_SW
1K
R601
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
NC
BA0
BA1
CLK
CKE
CS
RAS
CAS
WE
DQM0
DQM1
DQM2
DQM3
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
VDD
VDDQ
VSS
VSSQ
SDRAM-64MBX32
86 PIN TSOP
MT48LC2M32B2TG-5

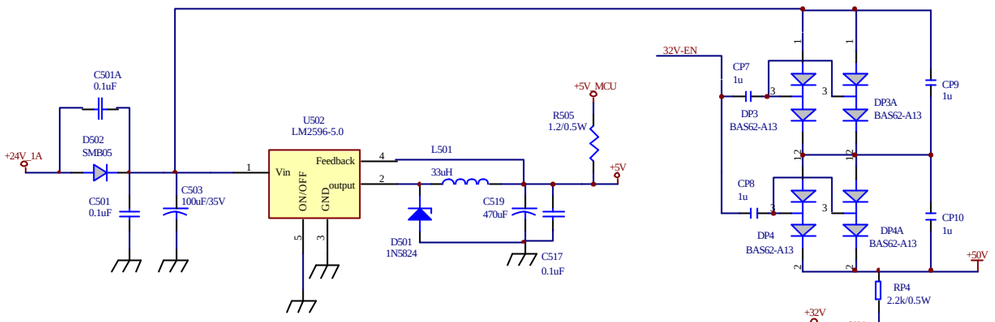
+2.5V_DDR
R600
10K
FSVREF
R602
10K
GND

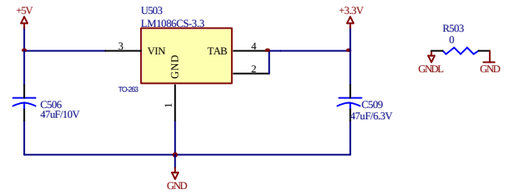
FSCLK+
FSCLK-
R603
150(140)


3.3VSDRAM1
3.3VSDRAM2
C618
C619
C620
C621
C622
C623
C624
C625
C626
C627
C628
C629
0.1uF
GND


OCMDATA[0..7]
OCMDATA[0..7]
OCMADDR[0..19]
OCMADDR[0..19]
U801
29LV800BT
+3.3V_DIG
37
13
14
VCC
VPP
WP#
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BYTE#
A-DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
A20/NC
A19/NC
RY/BY#
VSS
VSS
OE#
WE#
RST#
CE#
OCMADDR0
OCMDATA7
OCMDATA6
OCMDATA5
OCMDATA4
OCMDATA3
OCMDATA2
OCMDATA1
OCMDATA0
/OCM_WE
/OCM_RE
/ROM_CS
/RESET3.3V
R802
4.7K
R803
10K
+3.3V_DIG
C800
47uF/6.3V
C801
0.1uF
GND
RN800
10k
RN800A
10KX4
RN801
10K
RN801A
10K
Custom1
Custom2
Serial Interface Debug1
Serial Interface Debug2
Serial Interface Debug3
R804 0
R805 0
R806 0
R807 NC
BOOTSTRAP HEADER
OPEN=1
SHUNTED=0
INT_OSC
8-BIT_FLASH2
R800 10K 8-bit_flash1
R801 10K 8-bit_flash3
10: LOW (Use TCLK)
11: LOW (set all display output to '0')
12: LOW
13: LOW(disable serial interface debug)
14: LOW
15: LOW
16: HIGH (use crystal)
17: LOW (8bit bus with OCM access external ROM)
18: HIGH
19: LOW

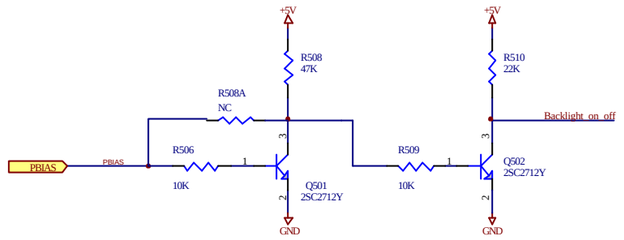

R519 NC
R521A NC
R521 NC
U501
LM2596-5.0
+12V_3A
C500
470uF
C502
0.1uF
R502
47K
Vin
ON/OFF
GND
Feedback
output
L500
33uH
D500
1N5824
C504
470uF
C502A
0.1uF
TP504
Panel_Power
C505
0.1uF
GNDL
R501
10K
PPWR
Q500
2SC2712Y
GND

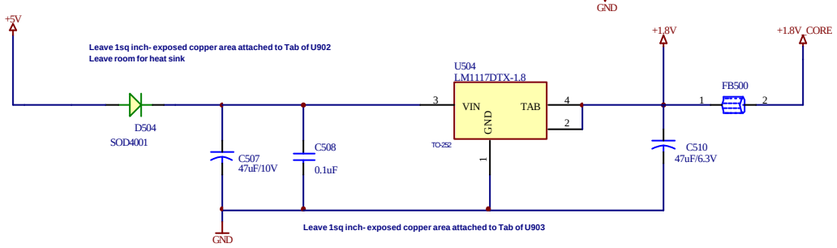

C501A
0.1uF
D502
SMB05
+24V_1A
C501
0.1uF
C503
100uF/35V
U502
LM2596-5.0
Vin
ON/OFF
GND
Feedback
output
L501
33uH
D501
1N5824
+5V_MCU
R505
1.2/0.5W
+5V
C519
470uF
C517
0.1uF
32V-EN
CP7
1u
DP3
BAS62-A13
DP3A
BAS62-A13
CP9
1u
CP8
1u
DP4
BAS62-A13
DP4A
BAS62-A13
CP10
1u
+50V
RP4
2.2k/0.5W
+32V
CP21
50V100uF
DP2
UPC574
CP31
0.1uF
GND

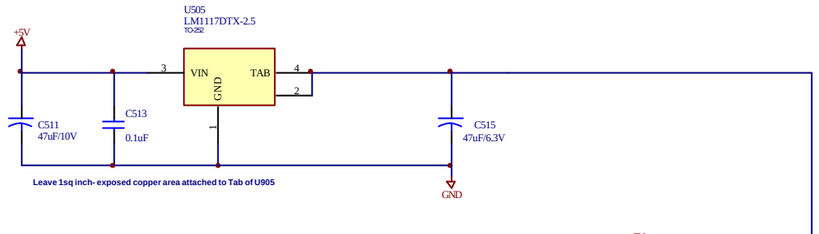

+5V
U503
LM1086CS-3.3
VIN
GND
TAB
TO-263
+3.3V
C506
47uF/10V
C509
47uF/6.3V
GND

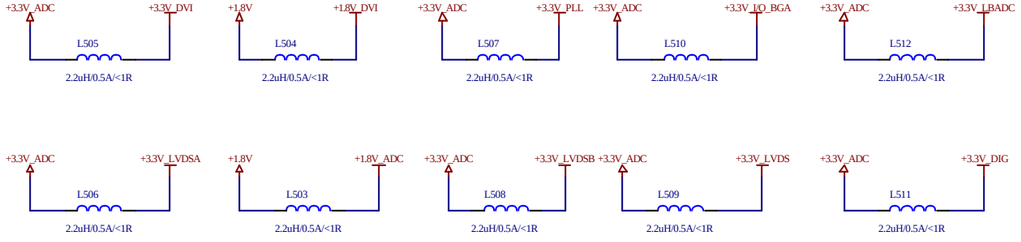
R503
0
GNDL
GND

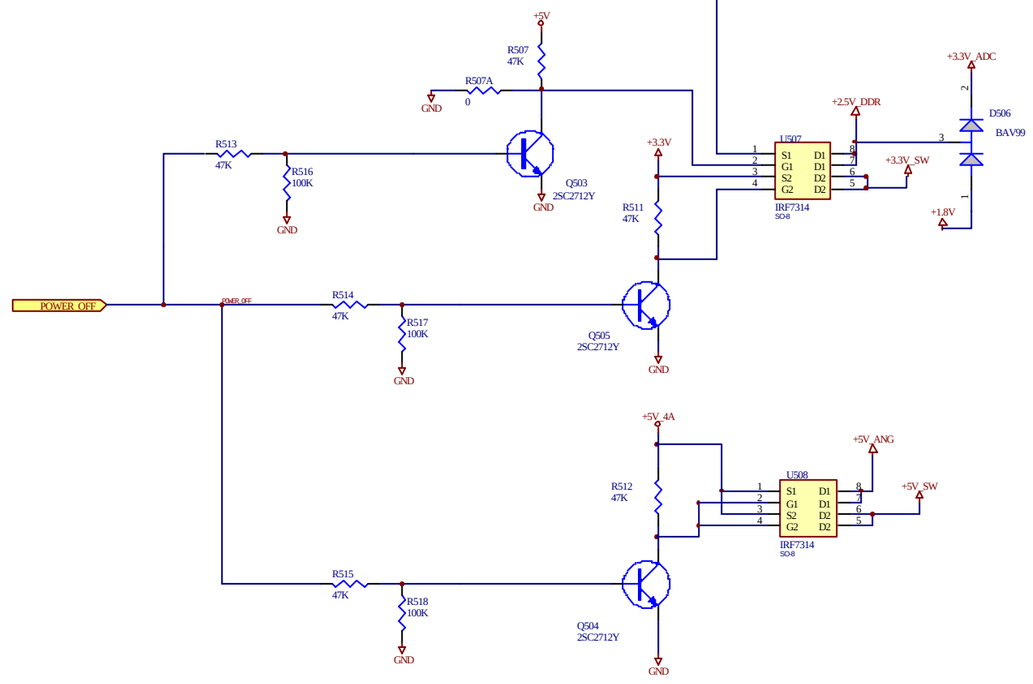
R504
0
GNDL
GND

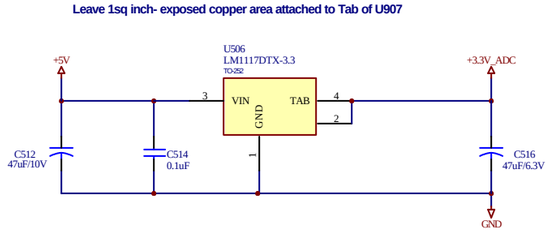

+5V
R508
47K
R508A
NC
R510
22K
Backlight_on_off
PBIAS
R506
10K
Q501
2SC2712Y
R509
10K
Q502
2SC2712Y
GND

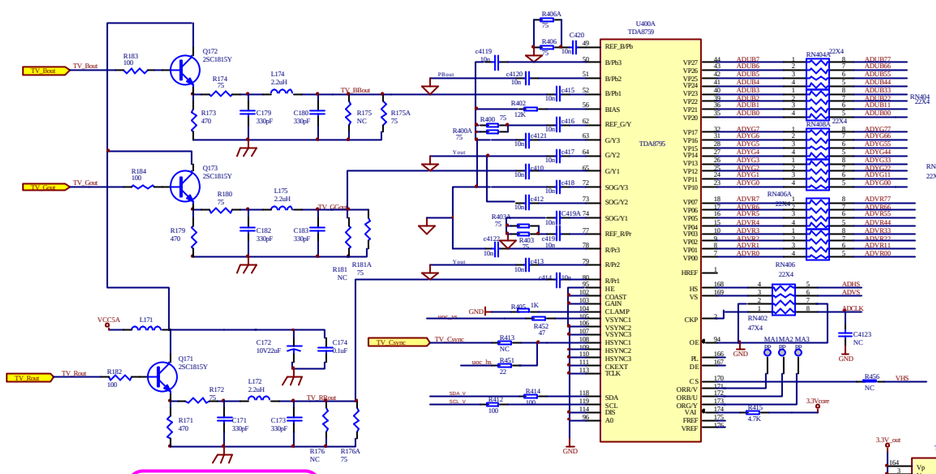

+5V
Leave 1sq inch- exposed copper area attached to Tab of U902
Leave room for heat sink
D504
SOD4001
U504
LM1117DTX-1.8
VIN
GND
TAB
TO-252
+1.8V
FB500
+1.8V_CORE
C507
47uF/10V
C508
0.1uF
C510
47uF/6.3V
GND
Leave 1sq inch- exposed copper area attached to Tab of U903

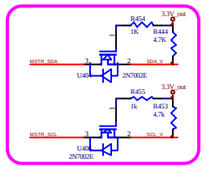

U505
LM1117DTX-2.5
TO-252
+5V
VIN
GND
TAB
C511
47uF/10V
C513
0.1uF
C515
47uF/6.3V
GND
Leave 1sq inch- exposed copper area attached to Tab of U905

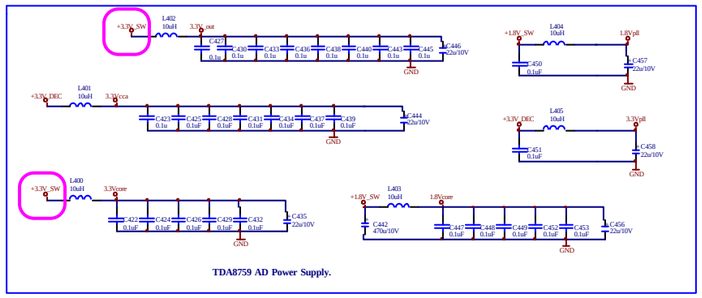

+3.3V_ADC
+3.3V_DVI
L505
2.2uH/0.5A/<1R
+1.8V
+1.8V_DVI
L504
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_PLL
L507
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_IO_BGA
L510
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_LBADC
L512
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_LVDSA
L506
2.2uH/0.5A/<1R
+1.8V
+1.8V_ADC
L503
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_LVDSB
L508
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_LVDS
L509
2.2uH/0.5A/<1R
+3.3V_ADC
+3.3V_DIG
L511
2.2uH/0.5A/<1R


+5V
R507
47K
R507A
0
GND
R513
47K
R516
100K
GND
Q503
2SC2712Y
GND
+3.3V
R511
47K
U507
S1
G1
S2
G2
D1
D1
D2
D2
IRF7314
SO-8
+2.5V_DDR
+3.3V_ADC
D506
BAV99
+3.3V_SW
+1.8V
POWER_OFF
POWR_OFF
R514
47K
R517
100K
GND
Q505
2SC2712Y
GND
+5V_4A
R512
47K
U508
IRF7314
SO-8
+5V_ANG
+5V_SW
R515
47K
R518
100K
GND
Q504
2SC2712Y
GND

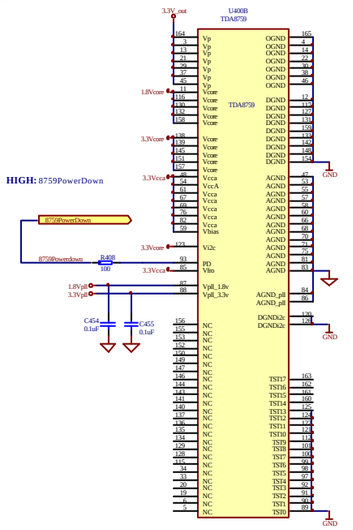

Leave 1sq inch- exposed copper area attached to Tab of U907
U506
LM1117DTX-3.3
TO-252
+5V
VIN
GND
TAB
+3.3V_ADC
C512
47uF/10V
C514
0.1uF
C516
47uF/6.3V
GND



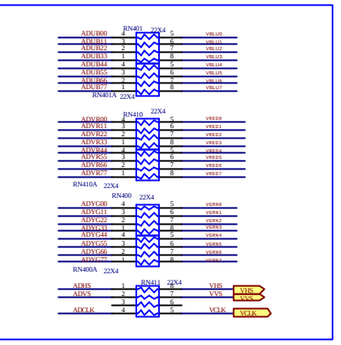




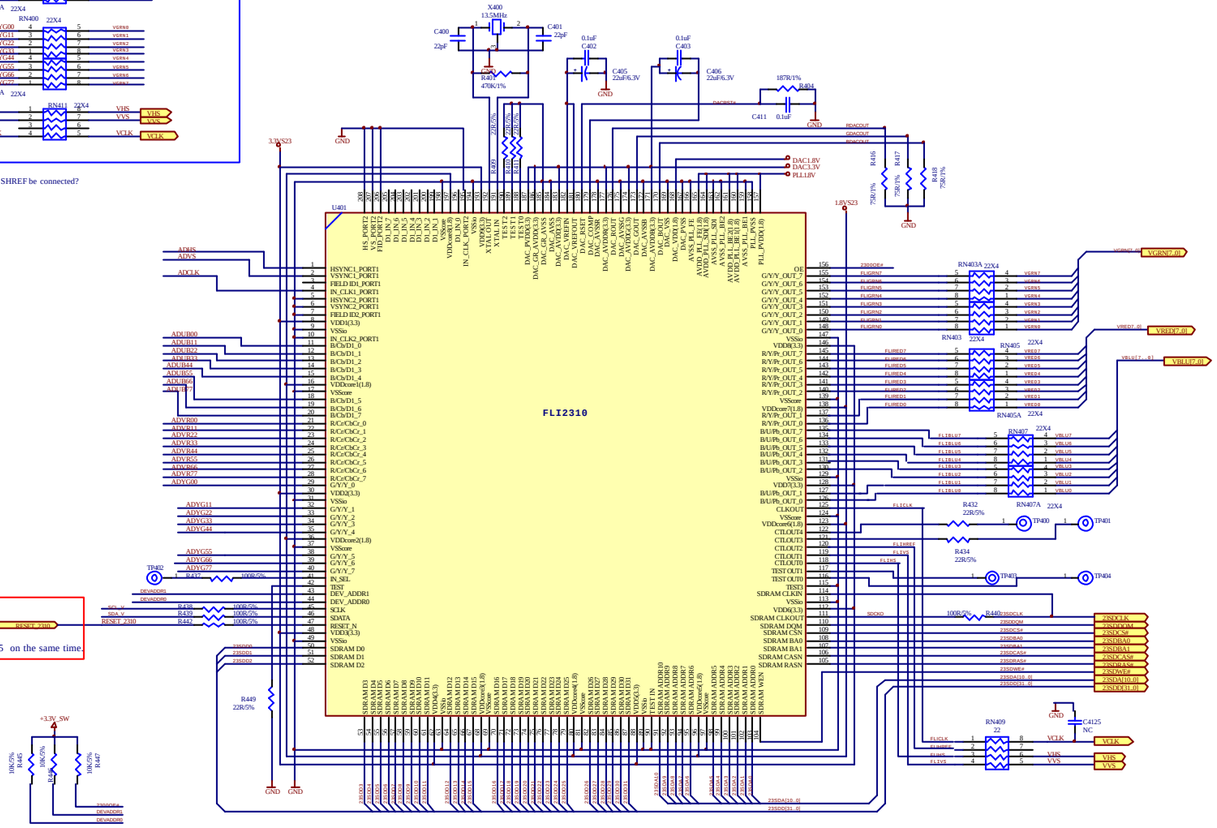
TDA8759 AD Power Supply.

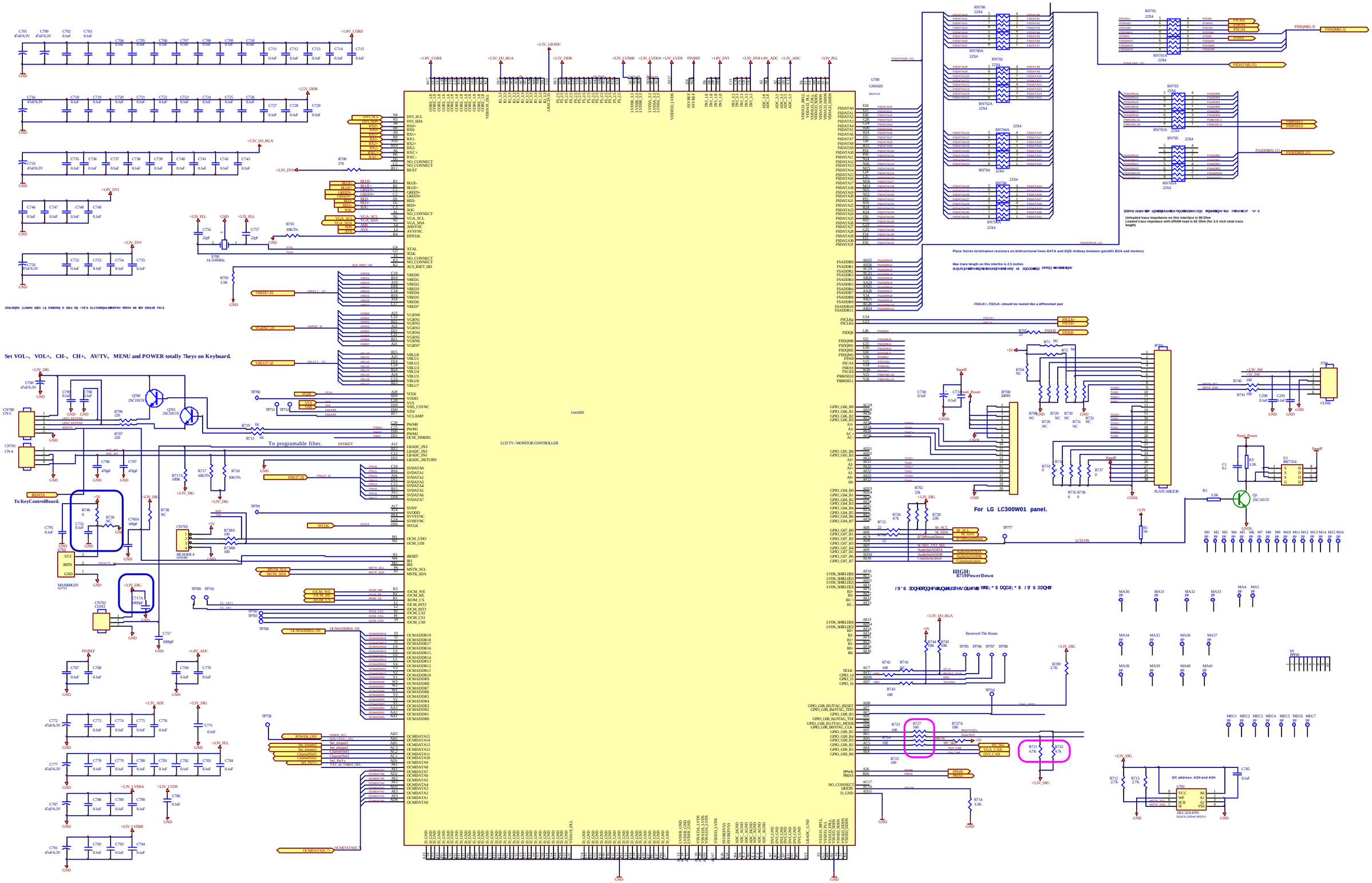


HIGH: 8759PowerDown

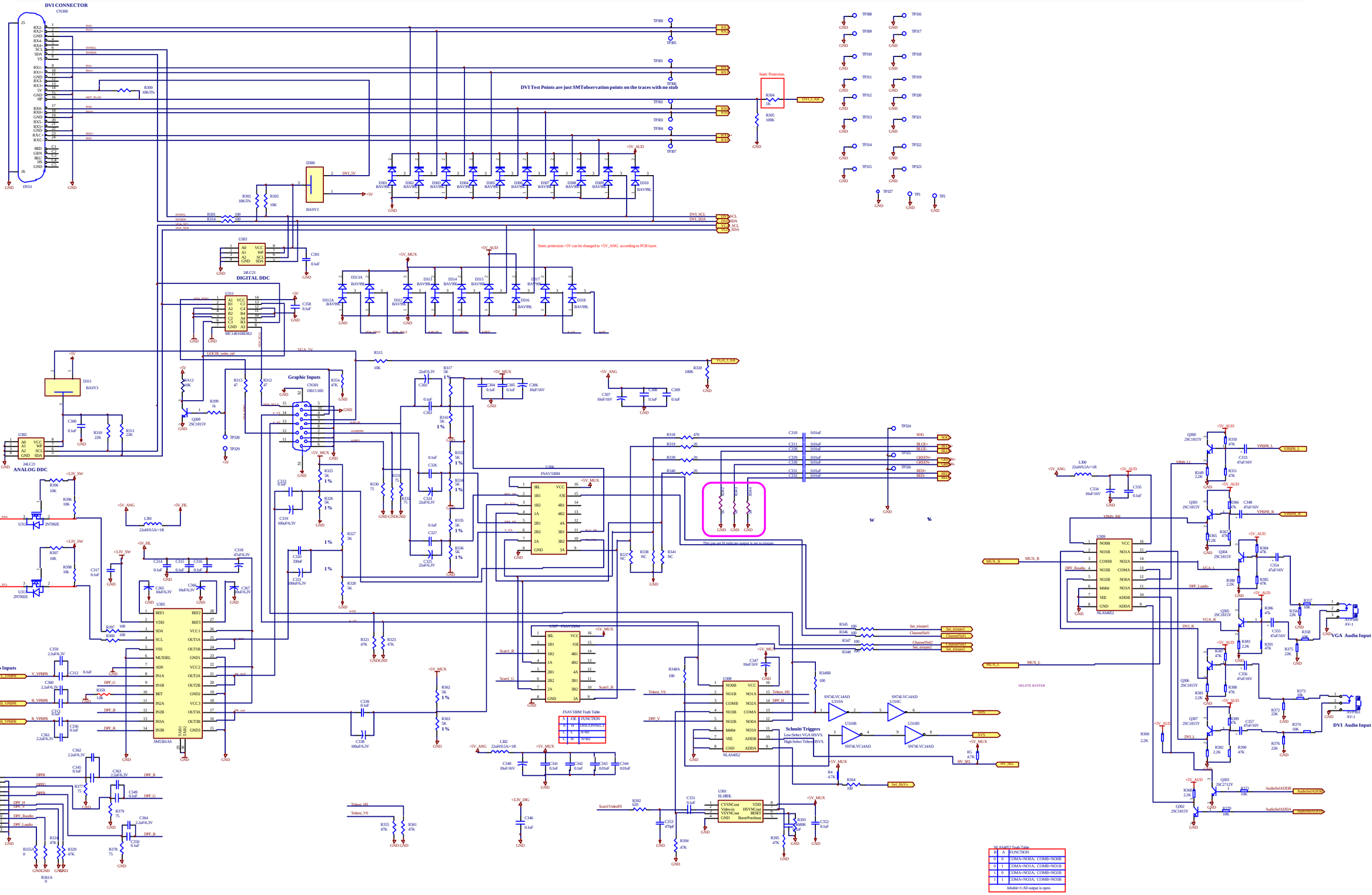


When FLI2300 is not installed,where should SHREF be connected?

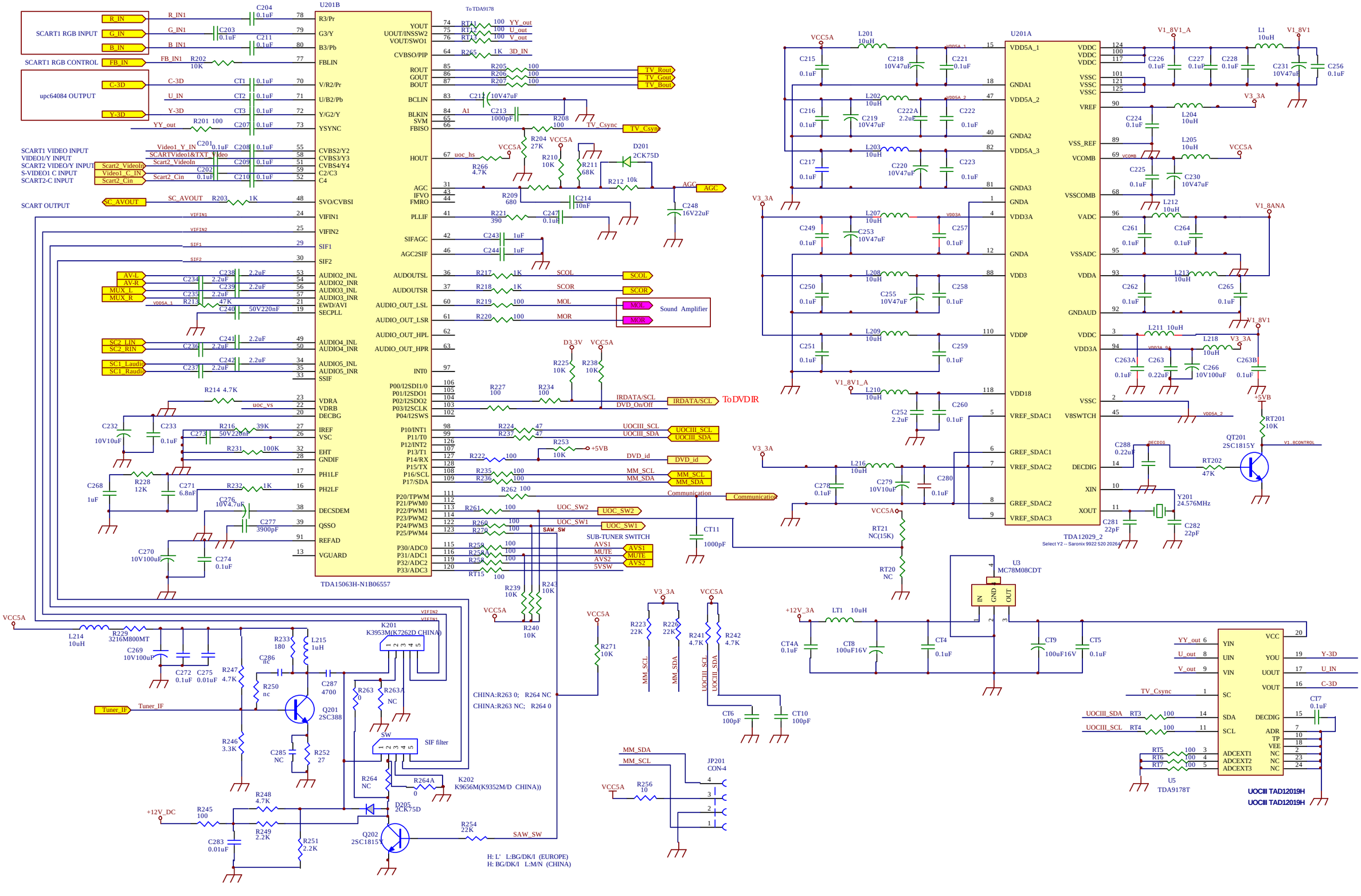


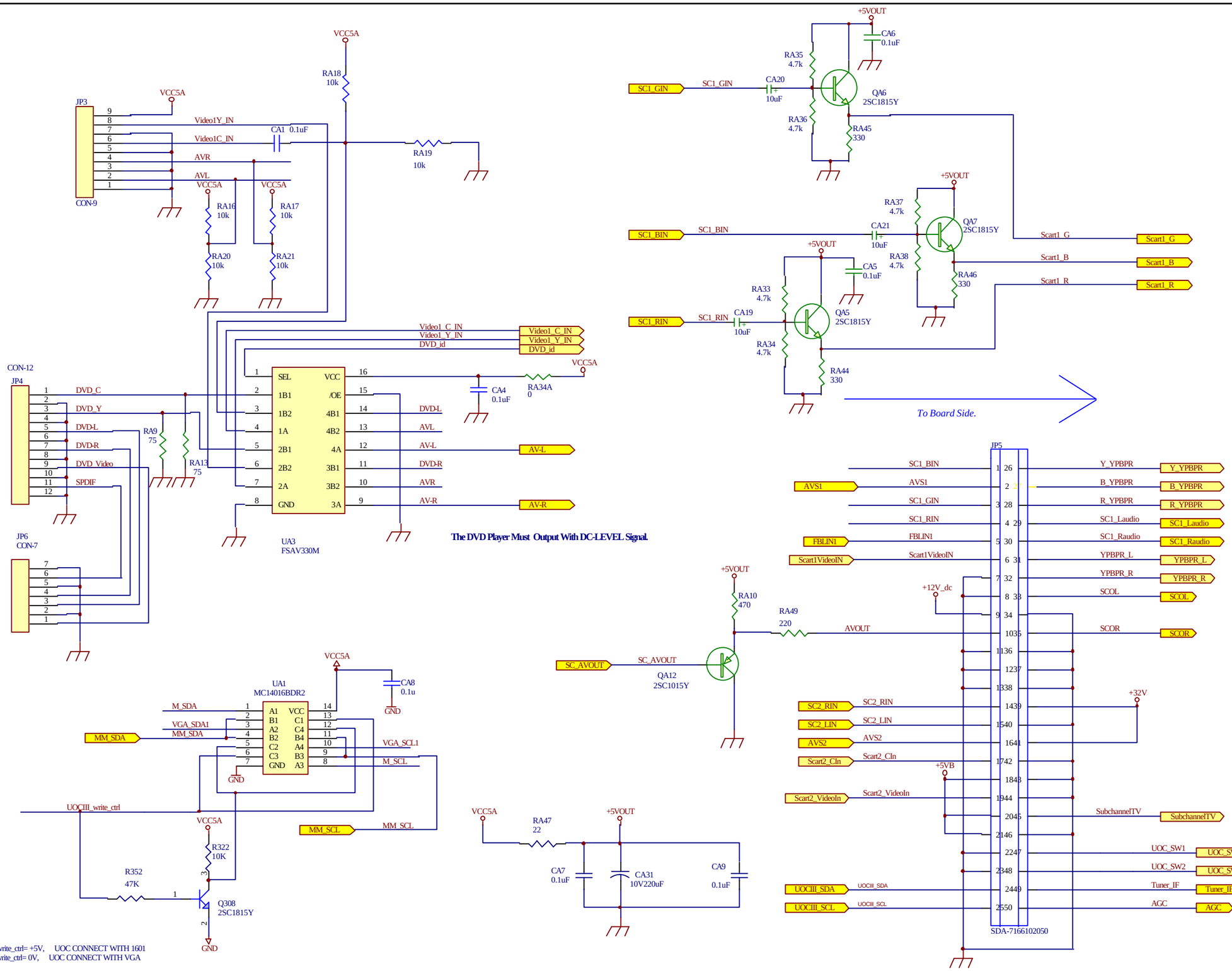


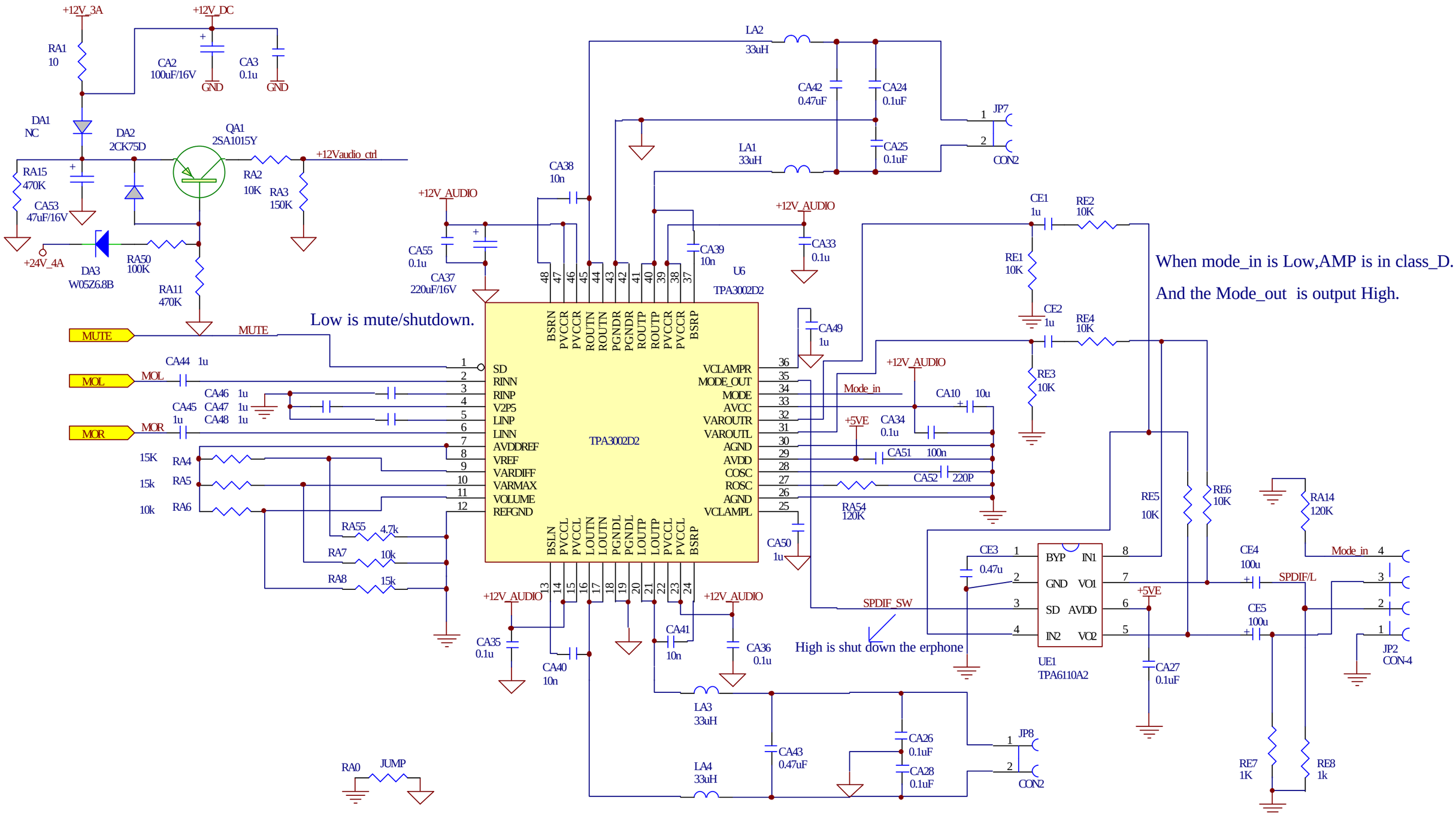
Model No.: LCT-32CHSTP
Version: 1.0

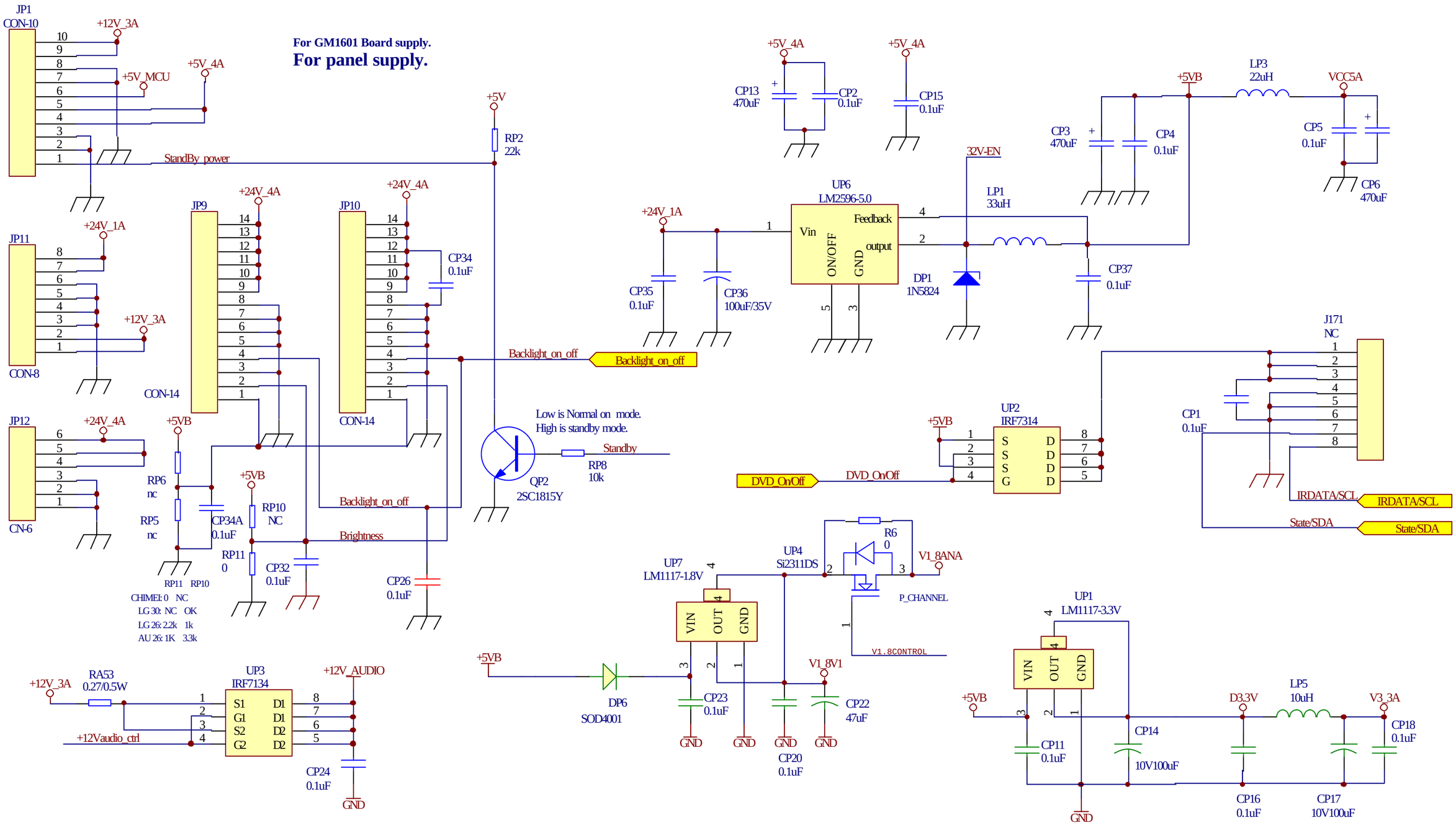


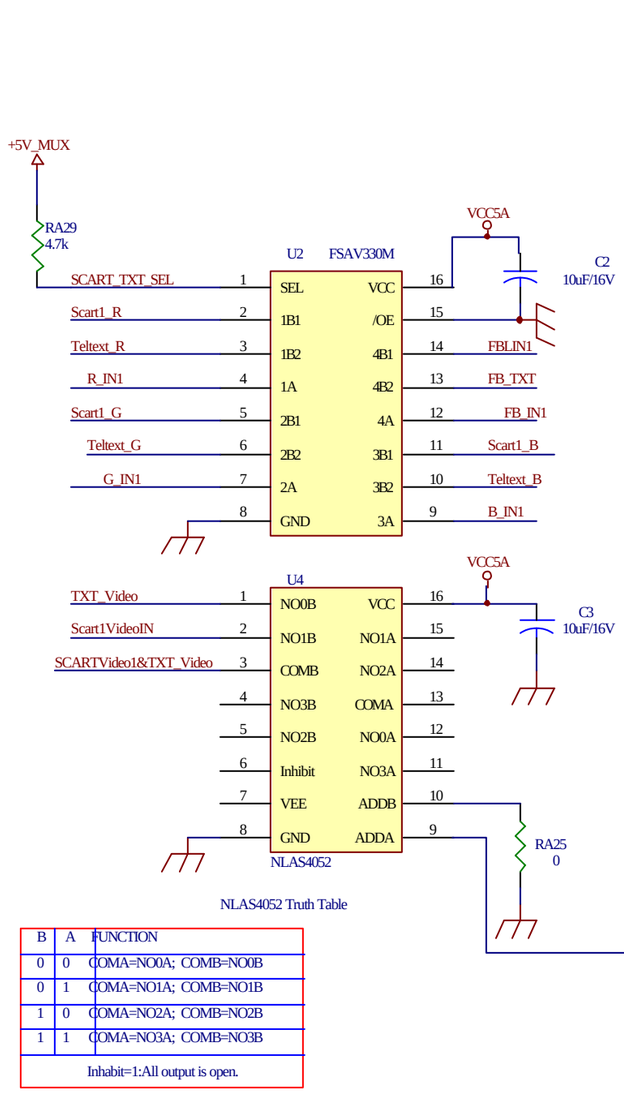
Model No.: LCT-32CHSTP
Version: 1.0


U201B
TDA15063H-N1B06557
To TDA9178
SCART1 RGB INPUT
SCART1 RGB CONTROL
upc64084 OUTPUT
SCART1 VIDEO INPUT
VIDEO1/Y INPUT
SCART2 VIDEO/Y INPUT
S-VIDEO1 C INPUT
SCART2-C INPUT
SCART OUTPUT
SUB-TUNER SWITCH
Sound Amplifier
To DVD IR
U201A
TDA12029_2
Select Y2 -- Saronix 9922 520 20264
U3
MC78M08CDT
U5
TDA9178T
JP201
CON-4
K201
K3953M(K7262D CHINA)
K202
K9656M(K9352M/D CHINA))
Q201
2SC388
Q202
2SC1815Y
SIF filter
CHINA:R263 0; R264 NC
CHINA:R263 NC; R264 0
H: L' L:BG/DK/I (EUROPE)
H: BG/DK/I L:M/N (CHINA)
UOCIII TAD12019H
UOCIII TAD12019H


VCC5A
RA18
10k
JP3
CON-9
Video1Y_IN
Video1C_IN
AVR
AVL
CA1 0.1uF
RA19
10k
RA16
10k
RA17
10k
RA20
10k
RA21
10k
Video1_C_IN
Video1_Y_IN
DVD_id
CON-12
JP4
DVD_C
DVD_Y
DVD-L
DVD-R
DVD_Video
SPDIF
RA9
75
RA13
75
SEL
1B1
1B2
1A
2B1
2B2
2A
GND
VCC
/OE
4B1
4B2
4A
3B1
3B2
3A
CA4
0.1uF
RA34A
0
DVD-L
AVL
AV-L
DVD-R
AVR
AV-R
UA3
FSAV330M
JP6
CON-7
The DVD Player Must Output With DC-LEVEL Signal.
+5VOUT
CA6
0.1uF
RA35
4.7k
SC1_GIN
CA20
10uF
QA6
2SC1815Y
RA36
4.7k
RA45
330
RA37
4.7k
SC1_BIN
CA21
10uF
QA7
2SC1815Y
RA38
4.7k
RA46
330
Scart1_G
Scart1_B
Scart1_R
CA5
0.1uF
RA33
4.7k
SC1_RIN
CA19
10uF
QA5
2SC1815Y
RA34
4.7k
RA44
330
To Board Side.
JP5
SC1_BIN
AVS1
SC1_GIN
SC1_RIN
FBLIN1
Scart1VideoIN
Y_YPBPR
B_YPBPR
R_YPBPR
SC1_Laudio
SC1_Raudio
YPBPR_L
YPBPR_R
SCOL
SCOR
+12V_dc
SC2_RIN
SC2_LIN
AVS2
Scart2_CIn
Scart2_VideoIn
+32V
+5VB
SubchannelTV
UOC_SW1
UOC_SW2
Tuner_IF
AGC
UOCIII_SDA
UOCIII_SCL
SDA-7166102050
+5VOUT
RA10
470
RA49
220
AVOUT
SC_AVOUT
QA12
2SC1015Y
UA1
MC14016BDR2
M_SDA
VGA_SDA1
MM_SDA
VGA_SCL1
M_SCL
MM_SCL
CA8
0.1u
GND
UOCIII_write_ctrl
R322
10K
R352
47K
Q308
2SC1815Y
UOCIII_write_ctrl= +5V, UOC CONNECT WITH 1601
UOCIII_write_ctrl= 0V, UOC CONNECT WITH VGA
RA47
22
CA7
0.1uF
CA31
10V220uF
CA9
0.1uF


+12V_3A
+12V_DC
RA1
10
CA2
100uF/16V
CA3
0.1u
GND
GND
DA1
NC
DA2
2CK75D
QA1
2SA1015Y
+12Vaudio_ctrl
RA15
470K
CA53
47uF/16V
RA2
10K
RA3
150K
+24V_4A
DA3
W05Z6.8B
RA50
100K
RA11
470K
MUTE
MUTE
MOL
MOL
CA44 1u
MOR
MOR
CA45 1u
CA46 1u
CA47 1u
CA48 1u
15K
RA4
15k
RA5
10k
RA6
RA55 4.7k
RA7 10k
RA8 15k
RA0 JUMP
+12V_AUDIO
CA55
0.1u
CA37
220uF/16V
CA38
10n
CA39
10n
U6
TPA3002D2
BSRN PVCCR PVCCR ROUTN ROUTN PGNDR PGNDR ROUTP ROUTP PVCCR PVCCR BSRP
48 47 46 45 44 43 42 41 40 39 38 37
SD
RINN
RINP
V2P5
LINP
LINN
AVDDREF
VREF
VARDIFF
VARMAX
VOLUME
REFGND
VCLAMPR
MODE_OUT
MODE
AVCC
VAROUTR
VAROUTL
AGND
AVDD
COSC
ROSC
AGND
VCLAMPL
1 2 3 4 5 6 7 8 9 10 11 12
36 35 34 33 32 31 30 29 28 27 26 25
BSLN PVCCL PVCCL LOUTN LOUTN PGNDL PGNDL LOUTP LOUTP PVCCL PVCCL BSRP
13 14 15 16 17 18 19 20 21 22 23 24
LA2
33uH
LA1
33uH
CA42
0.47uF
CA24
0.1uF
CA25
0.1uF
JP7
1
2
CON2
+12V_AUDIO
CA33
0.1u
CA49
1u
CA50
1u
CA35
0.1u
CA40
10n
CA41
10n
CA36
0.1u
LA3
33uH
LA4
33uH
CA43
0.47uF
CA26
0.1uF
CA28
0.1uF
JP8
1
2
CON2
Low is mute/shutdown.
When mode_in is Low,AMP is in class_D.
And the Mode_out is output High.
Mode_in
CA10 10u
+5VE
CA34
0.1u
CA51 100n
CA52 220P
RA54
120K
SPDIF_SW
High is shut down the erphone
CE3
0.47u
UE1
TPA6110A2
BYP IN1
GND VO1
SD AVDD
IN2 VO2
1 2 3 4
8 7 6 5
CA27
0.1uF
CE1
1u
RE2
10K
RE1
10K
CE2
1u
RE4
10K
RE3
10K
RE5
10K
RE6
10K
RA14
120K
CE4
100u
SPDIF/L
CE5
100u
JP2
CON-4
RE7
1K
RE8
1k

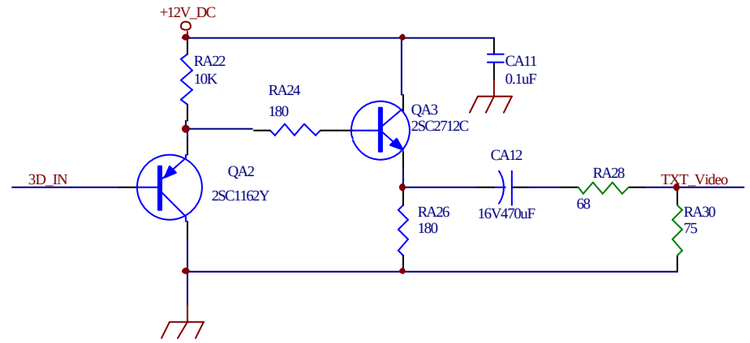

For GM1601 Board supply.
For panel supply.
JP1
CON-10
+12V_3A
+5V_MCU
+5V_4A
StandBy_power
+5V
RP2
22k
+5V_4A
CP13
470uF
CP2
0.1uF
+5V_4A
CP15
0.1uF
+5VB
LP3
22uH
VCC5A
CP3
470uF
CP4
0.1uF
CP5
0.1uF
CP6
470uF
32V-EN
LP1
33uH
UP6
LM2596-5.0
Vin
ON/OFF
GND
Feedback
output
+24V_1A
CP35
0.1uF
CP36
100uF/35V
DP1
1N5824
CP37
0.1uF
JP11
CON-8
+24V_1A
+12V_3A
JP9
CON-14
+24V_4A
JP10
CON-14
+24V_4A
CP34
0.1uF
Backlight_on_off
Backlight_on_off
Low is Normal on mode.
High is standby mode.
QP2
2SC1815Y
Standby
RP8
10k
J171
NC
CP1
0.1uF
IRDATA/SCL
IRDATA/SCL
State/SDA
State/SDA
UP2
IRF7314
+5VB
DVD_OnOff
DVD_OnOff
JP12
CN-6
+24V_4A
+5VB
RP6
nc
RP5
nc
CP34A
0.1uF
+5VB
RP10
NC
RP11
0
CP32
0.1uF
Backlight_on_off
Brightness
CP26
0.1uF
RP11 RP10
CHIMEI: 0 NC
LG 30: NC OK
LG 26: 2.2k 1k
AU 26: 1K 3.3k
UP7
LM1117-1.8V
VIN
OUT
GND
UP4
Si2311DS
R6
0
V1_8ANA
P_CHANNEL
V1.8CONTROL
+5VB
DP6
SOD4001
CP23
0.1uF
V1_8V1
CP22
47uF
CP20
0.1uF
UP1
LM1117-3.3V
VIN
OUT
GND
+5VB
CP11
0.1uF
CP14
10V100uF
D3.3V
LP5
10uH
V3_3A
CP18
0.1uF
CP16
0.1uF
CP17
10V100uF
RA53
0.27/0.5W
+12V_3A
+12Vaudio_ctrl
UP3
IRF7134
S1
G1
S2
G2
D1
D1
D2
D2
+12V_AUDIO
CP24
0.1uF
GND

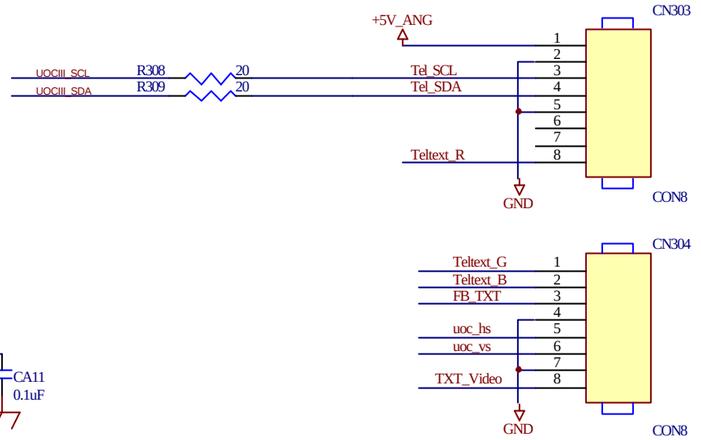


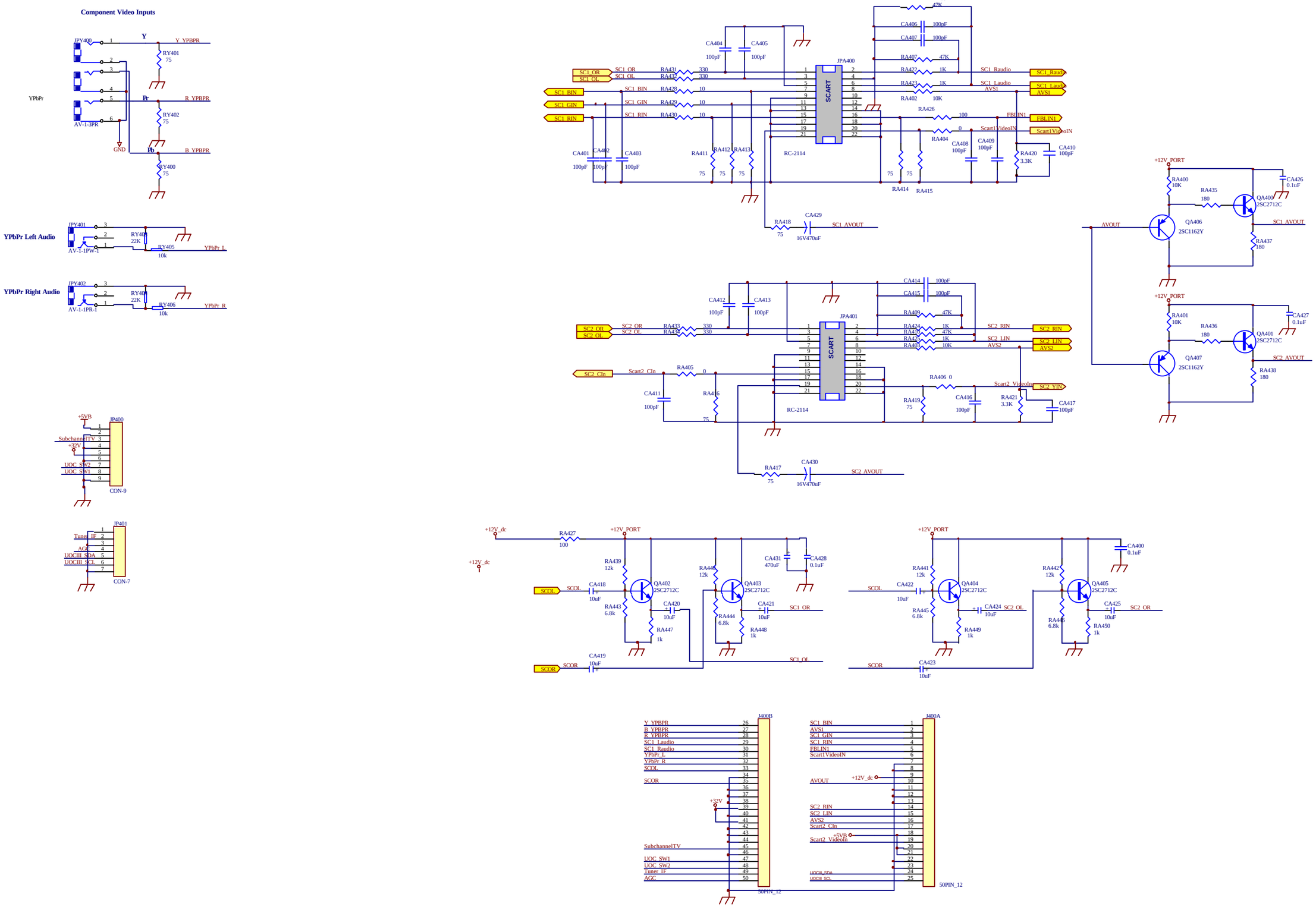
NLAS4052 Truth Table

B	A	FUNCTION
0	0	COMA=NO0A; COMB=NO0B
0	1	COMA=NO1A; COMB=NO1B
1	0	COMA=NO2A; COMB=NO2B
1	1	COMA=NO3A; COMB=NO3B

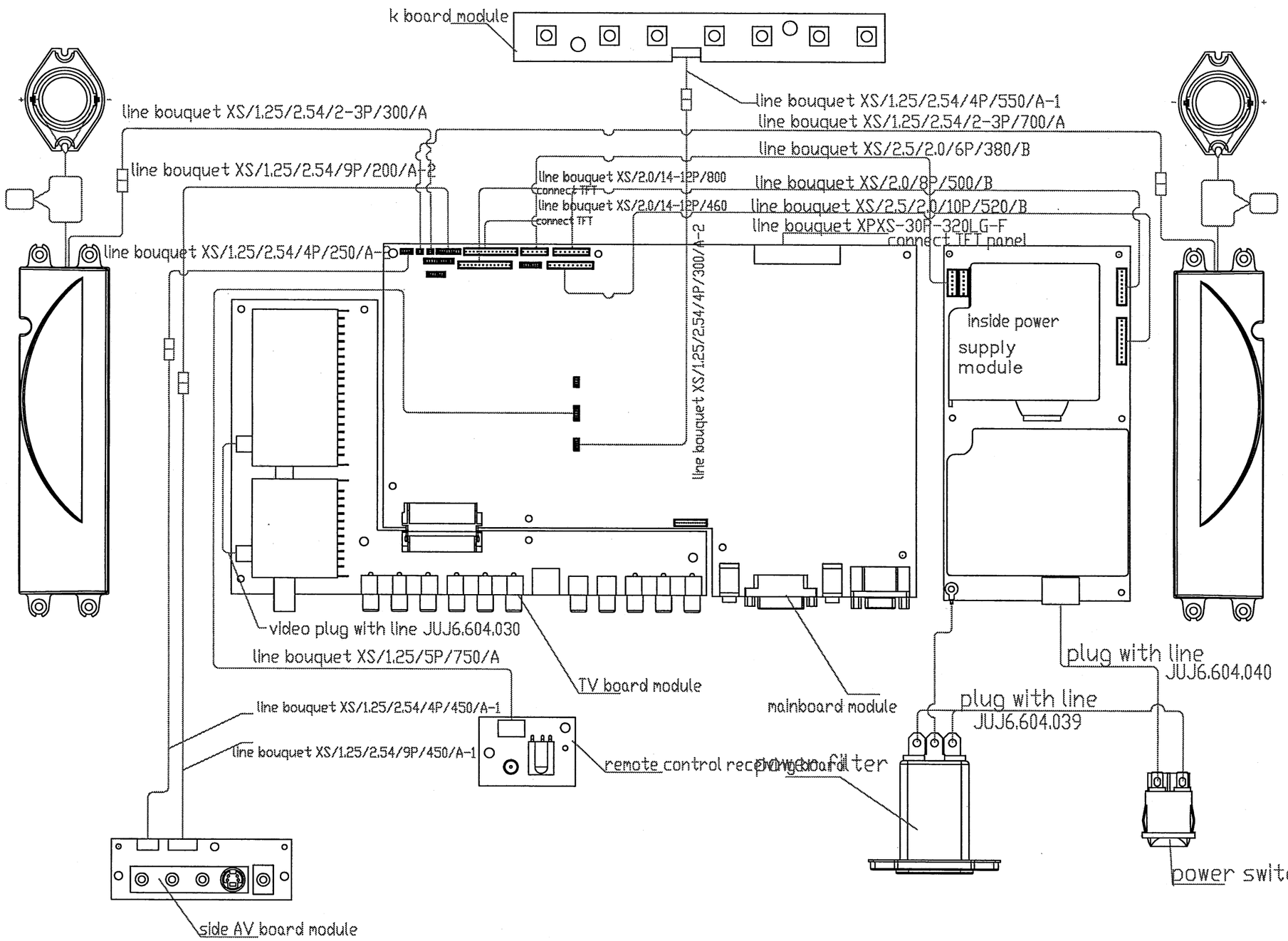
Inhibit=1:All output is open.



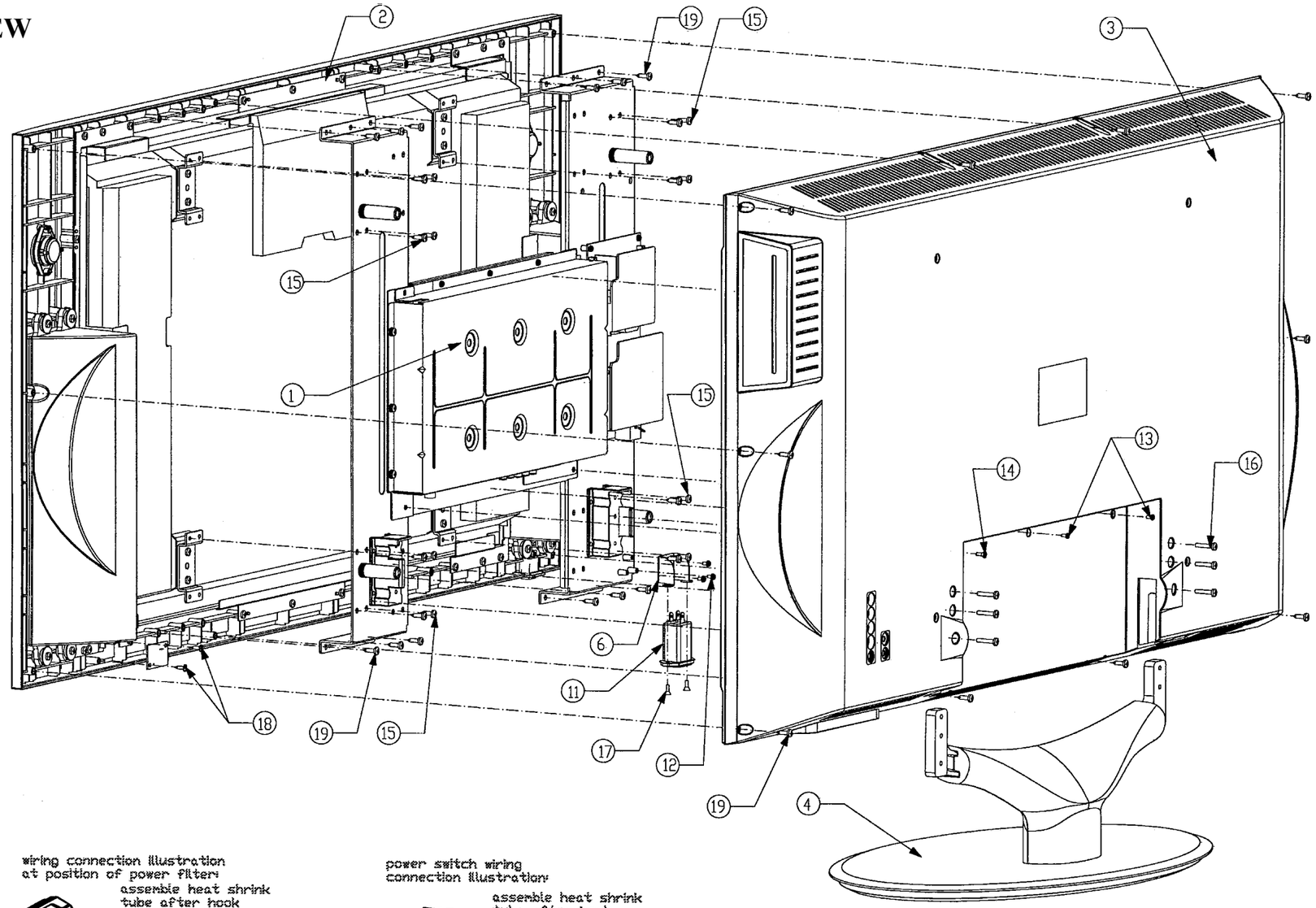


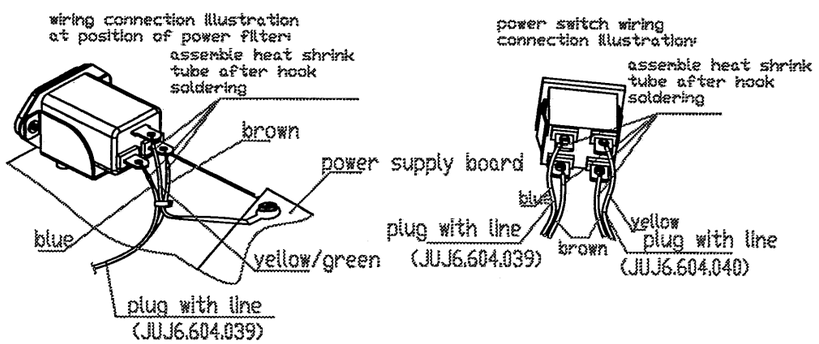

Component Video Inputs
JPY400
Y
Y_YPBPR
RY401
75
YPbPr
Pr
R_YPBPR
RY402
75
AV-1-3PR
GND
Pb
B_YPBPR
RY400
75
YPbPr Left Audio
JPY401
RY403
22K
AV-1-1PW-1
RY405
10k
YPbPr_L
YPbPr Right Audio
JPY402
RY404
22K
AV-1-1PR-1
RY406
10k
YPbPr_R
+5VB
JP400
SubchannelTV
+32V
UOC_SW2
UOC_SW1
CON-9
JP401
Tuner_IF
AGC
UOCIII_SDA
UOCIII_SCL
CON-7
JPA400
SCART
SC1_OR
SC1_OL
SC1_BIN
SC1_GIN
SC1_RIN
RA431
RA432
RA428
RA429
RA430
330
10
CA404
CA405
100pF
CA401
CA402
CA403
RA411
RA412
RA413
75
RC-2114
RA408
47K
CA406
CA407
100pF
RA407
RA422
RA423
1K
RA402
10K
SC1_Raudio
SC1_Laudio
AVS1
RA426
100
FBLIN1
Scart1VideoIN
RA404
0
CA408
CA409
CA410
RA420
3.3K
RA414
RA415
RA418
CA429
16V470uF
SC1_AVOUT
JPA401
SCART
SC2_OR
SC2_OL
SC2_CIn
RA433
RA434
RA405
CA411
RA416
CA412
CA413
CA414
CA415
RA409
RA424
RA410
RA425
RA403
SC2_RIN
SC2_LIN
AVS2
Scart2_CIn
Scart2_VideoIn
RA406 0
RA419
CA416
RA421
3.3K
CA417
RA417
CA430
SC2_AVOUT
+12V_PORT
QA400
2SC2712C
QA406
2SC1162Y
RA400
10K
RA435
180
CA426
0.1uF
RA437
180
QA401
2SC2712C
QA407
2SC1162Y
RA401
10K
RA436
180
CA427
0.1uF
RA438
180
AVOUT
+12V_dc
RA427
100
RA439
12k
RA443
6.8k
RA447
1k
QA402
2SC2712C
CA418
10uF
SCOL
CA419
10uF
SCOR
CA420
10uF
CA421
10uF
RA446
12k
RA444
6.8k
RA448
1k
QA403
2SC2712C
CA431
470uF
CA428
0.1uF
RA441
12k
RA445
6.8k
RA449
1k
QA404
2SC2712C
CA422
10uF
CA423
10uF
CA424 SC2_OL
10uF
RA442
12k
RA446
6.8k
RA450
1k
QA405
2SC2712C
CA400
0.1uF
CA425
10uF
SC2_OR
J400B
J400A
Y_YPBPR
B_YPBPR
R_YPBPR
SC1_Laudio
SC1_Raudio
YPbPr_L
YPbPr_R
SCOL
SCOR
SubchannelTV
UOC_SW1
UOC_SW2
Tuner_IF
AGC
SC1_BIN
AVS1
SC1_GIN
SC1_RIN
FBLIN1
Scart1VideoIN
SC2_RIN
SC2_LIN
AVS2
Scart2_CIn
Scart2_VideoIn
UOCIII_SDA
UOCIII_SCL
50PIN_12

WIRING DIAGRAM



EXPLODED VIEW





1. Connect each line bouquet and plug with line according to final wiring connection diagram.
2. Routing of the bouguet and plug with line is confirmed by professional technologist and paste adhensive tape at suitable position to fix them and require routing not dispersedness.
3. Conductive sponge is posted at back of TFT panel first. Then fasten it using chassis module.
4. Check each key flexible or not, switch reliable or not, not permit block phenomenon to appear. If has no problem, assemble back cover module.
5. After finish unit assembly, fix protect corner cushion on the four corner of front frame using blue adhensive tape.
6. After unit is passed examination, paste certification, DVD label and fragile label on the surface of back cover. Require position of pasting should be consistent.

PART LIST

NO	PART NAME
1	Chassis module
2	Front frame module
3	Back cover module
4	Pedestal module
5	Plug with line
6	Power bracket
11	Power filter
12	Screw M3x6
13	Screw M3x8
14	Screw M3x8
15	Screw M4x8
16	Screw M4x20
17	Screw M3x10
18	Screw M3x12
19	Screw 6x16

AKIRA
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